Multi Gigabit PCB/Channel Analysis

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In general, we should make sure that our channel performs well in the following:

- Channel frequency response (IL, ILD, ICR, RL…) meets relevant standards, chip-to-chip and per-board. This can be done on the S-parameters from a PCB EM simulation results or on measured (with VNA) prototype.
- Channel time domain TDR response should be smooth enough without too much impedance peaks.
- Time domain Eye simulation with many crosstalk aggressors and IBIS-AMI models meets the RX chip eye height/width requirements after DFE (in Auto mode)
- Time domain Eye BERT scan on the prototype system with either an Oscilloscope, or with an on-chip built-in Eye measurement feature.

Frequency domain:

For Ethernet interfaces (1-40G, like 10GBase-KR, 40GBase-KR4…) The IEEE802.3ap standard Annex 69B provides frequency domain channel characteristics limits for chip to chip full channel. These limits are defined up to a certain frequency that is actually quite low. When we do the PCB extraction to S-parameters, we have to use a 3D FW simulator that properly accounts for the GND-plane discontinuities like nearby via-antipads.

The limits in IEEE802.3ap are defined on:

- Differential Insertion loss versus frequency curve (IL). For 10G-KR it is 30dB at 6GHz and 80dB at 9GHz.
- Fitted Attenuation (FA, compute from IL with moving average, center line of IL)
- Insertion loss deviation (ILD). ILD(f)=IL(f) – FA(f), compute with Matlab. It is hard for the RX-DFE to compensate for this.
- Return loss (RL).
- Insertion loss to crosstalk ratio (ICR). FEXT or |NEXT(f, dB)|-|IL(f, dB)|=ICR(f). Practically have at least 23dB between IL(f) and FEXT or NEXT(f) at data rate /2.

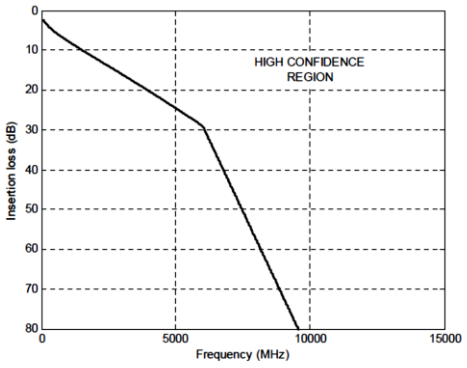


Figure 69B–5—Insertion loss limit for 10GBASE-KR

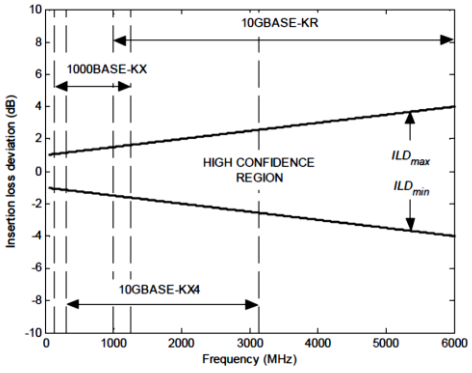


Figure 69B–6—Insertion loss deviation limits

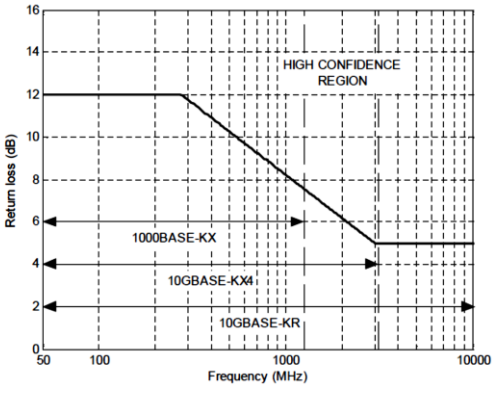


Figure 69B–7—Return loss limit

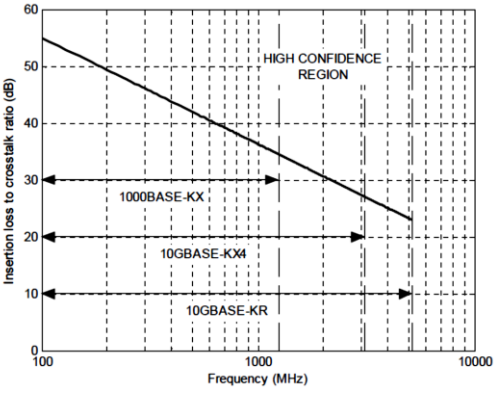
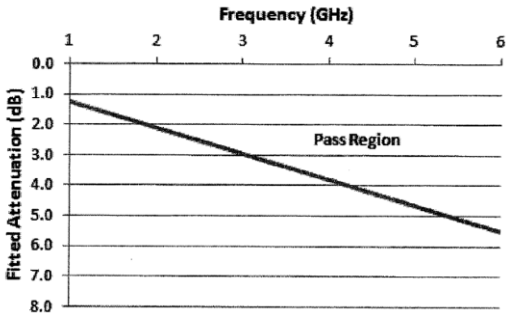


Figure 69B–8—Insertion loss to crosstalk ratio limit

For partial channel, there are some specifications defined by form factor standards, for example:
- PICMG3.1 page 100, ATCA front board's backplane interface has FA and ICR (and nothing else) defined.
- PICMG3.1, ATCA full channel FA/IL/ILD/ICR and mode conversion defined.
- SFF8431 provides host board (to SFP+ module pins) specs for SDD21(f), SCC21(f), NEXT(f)

Figure 5-36 Fitted attenuation limit for LCLASS 0011b signal paths in Front Board



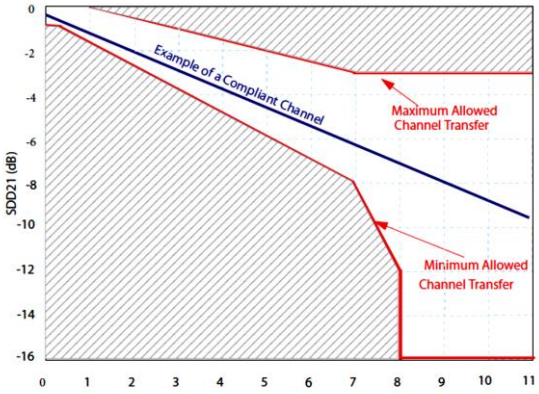


Figure 33 Example of SFI Host Recommended Channel

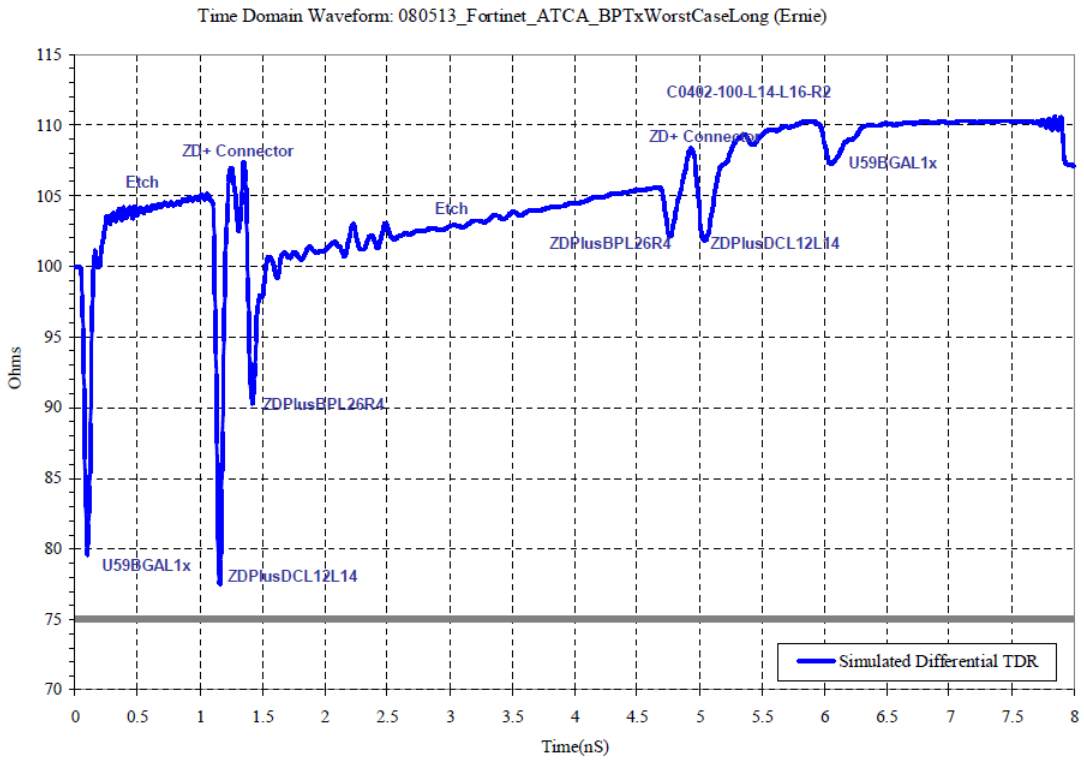
For 25G+ signalling on 100G Ethernet a new standard the IEEE802.3bj is being published in Q2-2014.

Individual elements (like connector, BGA fanout, AC-CAP) should also meet some arbitrary practical requirements:

- Crosstalk: NEXT and FEXT should be below -40dB at data rate /2.
- Return Loss: Practically have at -17.5dB or below at data rate /2.

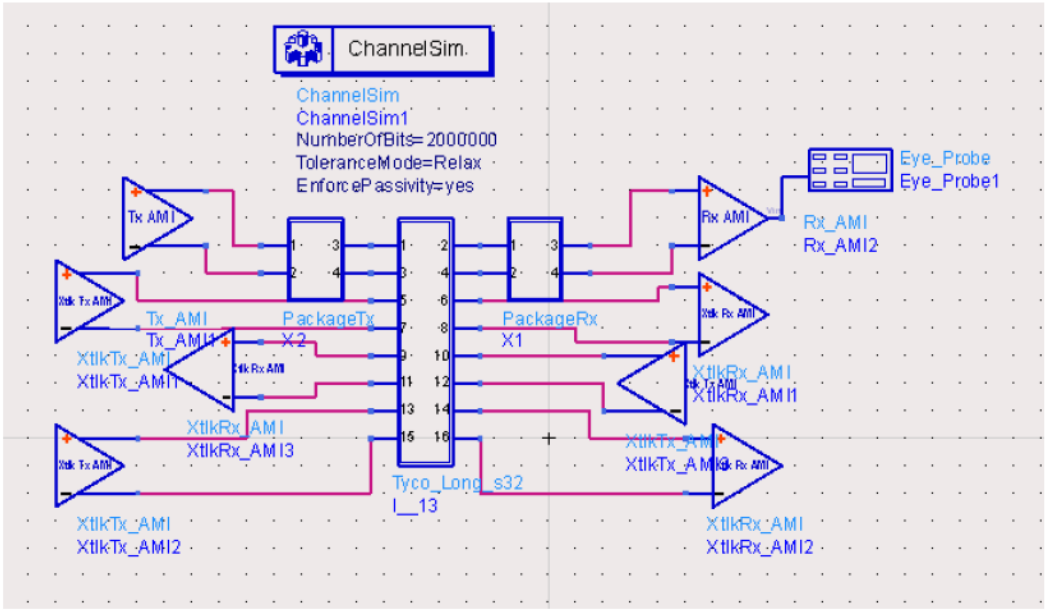
Time Domain channel:

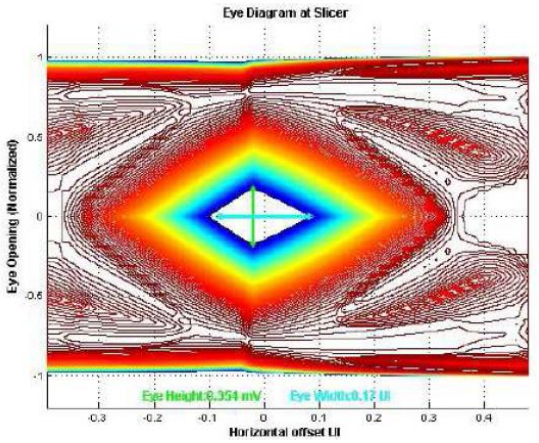
The TDR response of the channel shows impedance discontinuities as peaks and valleys. They can be identified by their time-position, after calculating time-to-distance and then measuring the distance of the discontinuity from the start port on the PCB. Try to optimize layout to reduce the surges to <<+/-10%. The negative valleys show low impedance points, often via transitions and breakout. The positive peaks show high impedance, for example GND plane undercut by nearby antipads. All of the impedance discontinuities (peak/valley) directly cause reflection, indirectly ILD and crosstalk.



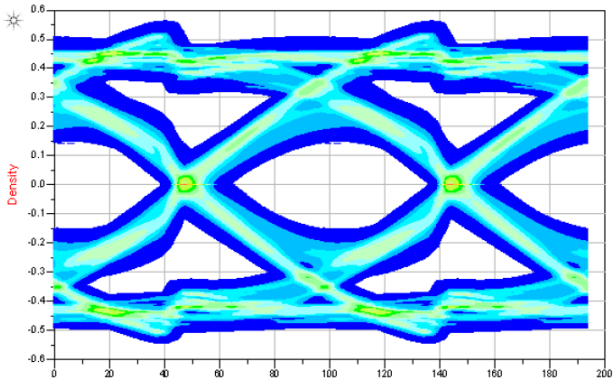
Time domain Eye simulation:

This is simple channel simulation using IBIS-AMI models. We can use Agilent ADS, Ansoft NExxim, Hyperlynx, StatEye+MAtlab or Broadcom LinkEye simulators. The BCM LinkEye uses 8 crosstalk aggressors, that measurably reduces the eye. The eye width and height after the DFE (part of IBIS-AMI model) has to meet the receiver datasheet requirements. The LinkEye also tells the freq-domain analysis results against IEEE802.3ap in a table.





Broadcom LinkEye



Agilent ADS

Time domain Eye BERT scan on the prototype system

Use either an Oscilloscope (BW=2.5xDataRate), or use the on-chip built-in Eye measurement feature. The second option is 1000x cheaper solution, and more accurate as no additional elements get introduced into the channel. Avago, Altera (Transceiver Toolkit), Broadcom, PLX (SDK) and others have it. Normally readable through a USB dongle (I2C, MDIO), or through software running on the DUT (requires software engineering to adjust to board design). The DUT has to be in PRBS gen/test mode with external loopback. We can display 3D(2D color or BW at fixed BER) BERT scan or 2D Bathtub curves.