LogiCORE™ IP SelectIO™ Interface Wizard v1.2

Getting Started Guide

UG700 (v1.2) December 2, 2009

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/16/09	1.1	Initial Xilinx release.
12/02/09	1.2	Updated tool versions. Added Phase Detector Interface Ports to Table 3-1. Added “Phase Detector” in Chapter 4. Replaced the following: IODELAY with IODELAY2; ISERDES with ISERDES2; OSERDES with OSERDES2; IDDR with IDDR2; ODDR with ODDR2.

Table of Contents

About This Guide

The guide provides information about the Xilinx® LogiCORE™ IP SelectIO™ Interface Wizard core. This guide walks you through using the graphical user interface (GUI) and explains how to use the provided example design and test bench.

Guide Contents

This guide contains the following chapters:

- Preface, "About this Guide" introduces the organization and purpose of this guide, a list of additional resources, and the conventions used in this document.
- Chapter 1, "Introduction" describes the core and related information, including recommended design experience, additional resources, technical support, and submitting feedback to Xilinx.
- Chapter 2, "Installation and Licensing" provides instructions for installing the LogiCORE IP SelectIO Interface Wizard in the Xilinx® CORE Generator™ tool.
- Chapter 3, "Core Architecture" describes the generated I/O circuit, including the datapath and clock generators.
- Chapter 4, "Generating the Core" provides complete information about the GUI, including detailed information about entering parameters to generate the desired I/O circuit.
- Chapter 5, "Detailed Example Design" describes the provided example design and test bench.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support/mysupport.htm.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *User Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Dark Shading	Items that are not supported or reserved	This feature is not supported
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	**`lowpwr =`**{**`on`**|**`off`**}
Vertical bar |	Separates items in a list of choices	**`lowpwr =`**{**`on`**|**`off`**}
Angle brackets < >	User-defined variable or in code samples	<directory name>

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *block_name loc1 loc2 ... locn;*
Notations	The prefix '0x' or the suffix 'h' indicate hexadecimal notation	A read of address 0x00112975 returned 45524943h.
	An '_n' means the signal is active low	**`usr_teof_n`** is active low.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

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Chapter 1

Introduction

This chapter introduces the SelectIO™ Interface Wizard core and provides related information, including recommended design experience, additional resources, technical support, and submitting feedback to Xilinx. The SelectIO Interface Wizard core generates source code to implement an I/O circuit matched to your requirements and is designed to support both Verilog and VHDL design environments. In addition, the example design delivered with the core is provided in both Verilog and VHDL.

About the Core

The SelectIO Interface Wizard core is a Xilinx® CORE Generator™ IP core supporting the Spartan-6 SelectIO Interface, included in the latest IP Update on the Xilinx IP Center.

Recommended Design Experience

The SelectIO Interface Wizard is designed to be used by those will some level of experience with Xilinx I/Os. It is the Xilinx recommended method to create your I/O circuit. Advanced users can modify the provided source code. Although the SelectIO Interface Wizard provides a fully verified solution, understanding the Xilinx I/O primitives will aid users in making design trade-off decisions.

Related Xilinx Documents

UG381: *Spartan-6 FPGA SelectIO Resources User Guide*

UG382: *Spartan-6 FPGA Clocking Resources User Guide*

DS709: *LogiCORE IP Clocking Wizard Data Sheet*

UG521: *LogiCORE IP Clocking Wizard Getting Started Guide*

ISE® documentation at http://www.xilinx.com/ise

Additional Core Resources

For more information on the SelectIO Interface Wizard, do the following

1. Go to the IP center (http://www.xilinx.com/ipcenter/)
2. Under Browse for Intellectual Property, select the "+" sign next to By Function
3. Select FPGA Features and Design. The SelectIO Interface Wizard documents will be listed.

Technical Support

For technical support, go to www.xilinx.com/support. Questions are routed to a team with expertise using the SelectIO Interface Wizard core.

Xilinx will provide technical support for use of this product as described in the *LogiCORE IP SelectIO Interface Wizard v1.2 Getting Started Guide*. Xilinx cannot guarantee timing, functionality, or support of this product for designs that do not follow these guidelines.

Feedback

Xilinx welcomes comments and suggestions about the SelectIO Interface Wizard core and the accompanying documentation.

SelectIO Interface Wizard

For comments or suggestions about the SelectIO Interface Wizard, please submit a WebCase from www.xilinx.com/support/clearexpress/websupport.htm. Be sure to include the following information:

- Product name
- Core version number
- Explanation of your comments

Document

For comments or suggestions about the SelectIO Interface Wizard core, please submit a WebCase from www.xilinx.com/support/clearexpress/websupport.htm. Be sure to include the following information:

- Document title
- Document number
- Page number(s) to which your comments refer
- Explanation of your comments

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Chapter 2

Installation and Licensing

This chapter provides instructions for installing the LogiCORE IP SelectIO™ Interface Wizard in the Xilinx® CORE Generator™ tool. It is not necessary to obtain a license to use the Wizard.

Supported Tools and System Requirements

Operating Systems

Windows

- Windows XP Professional 32-bit/64-bit
- Windows Vista Business 32-bit/64-bit

Linux

- Red Hat Enterprise Linux WS v4.0 32-bit/64-bit
- Red Hat Enterprise Desktop v5.0 32-bit/64-bit (with Workstation Option)
- SUSE Linux Enterprise (SLE) desktop and server v10.1 32-bit/64-bit

Tools

- ISE® v11.4 software
- Mentor Graphics ModelSim: v6.4b and above
- Cadence IUS v8.1 -s009 and above
- Synopsys 2008.09 and above

Check the release notes for the required Service Pack; ISE Service Packs can be downloaded from www.xilinx.com/xlnx/xil_sw_updates_home.jsp?update=sp.

Before You Begin

Before installing the Wizard, you must have a MySupport account and the ISE 11.4 software installed on your system. If you already have an account and have the software installed, go to "Installing the Wizard", otherwise do the following:

1. Click **Login** at the top of the Xilinx home page then follow the onscreen instructions to create a MySupport account.
2. Install the ISE 11.4 software.

   For the software installation instructions, see the ISE Design Suite Release Notes and Installation Guide available in ISE software Documentation.

Installing the Wizard

The LogiCORE IP SelectIO Interface Wizard is included with the ISE 11.4 software. See *ISE CORE Generator IP Updates - Installation Instructions* for details about the installation of ISE 11.4 software.

Verifying Your Installation

Use the following procedure to verify that you have successfully installed the LogiCORE IP SelectIO Interface Wizard in the CORE Generator tool.

1. Start the CORE Generator tool.
2. The IP core functional categories appear at the left side of the window, as shown in Figure 2-1.

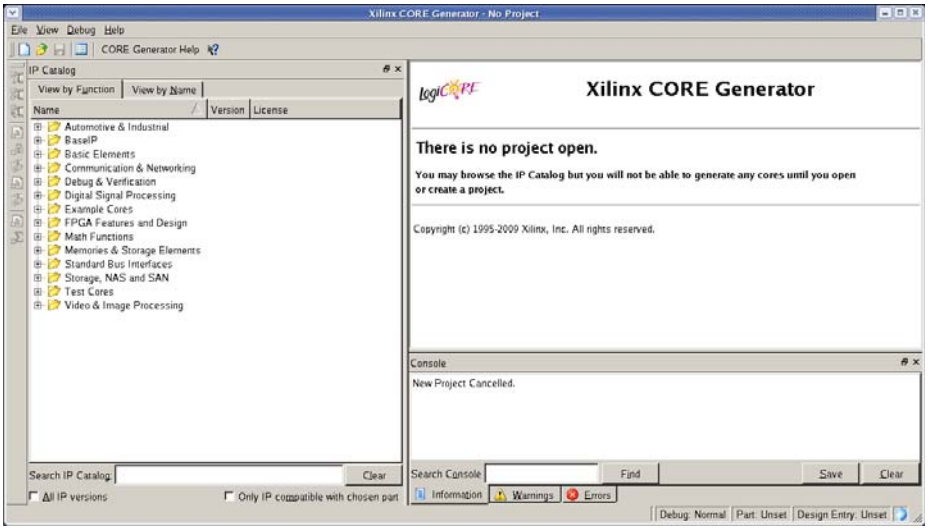

Figure 2-1: **CORE Generator Tool Window**

3. Click to expand or collapse the view of individual functional categories, or click the **View by Name** tab at the top of the list to see an alphabetical list of all cores in all categories.
4. Determine if the installation was successful by verifying that SelectIO Interface Wizard v1.1 appears at the following location in the Functional Categories list:
   `/FPGA Features and Design/IO Interfaces`

Chapter 3

Core Architecture

The SelectIO™ Interface Wizard provides source HDL which implements an I/O circuit for an input, output or bidirectional bus, including the buffer, any delay elements, serialization, registers, and the I/O clock driver. The circuit is designed in two major components: clock buffering and manipulation; and datapath, which is implemented per pin.

Clock Buffering and Manipulation

The wizard supports the use of a BUFG, BUFIO2, or BUFPLL for clocking the I/O logic. An example circuit illustrating a BUFIO2 primitive with input data is illustrated in Figure 3-1.

Insertion delay can be added for the input clock (except in the case of a BUFPLL, which is driven from a PLL_BASE in fabric).

For serialization or deserialization of the datapath, the slower divided fabric clock is created and/or aligned to the input clock on behalf of the user (except in the case of a BUFG, which does not support serialized/deserialized data).

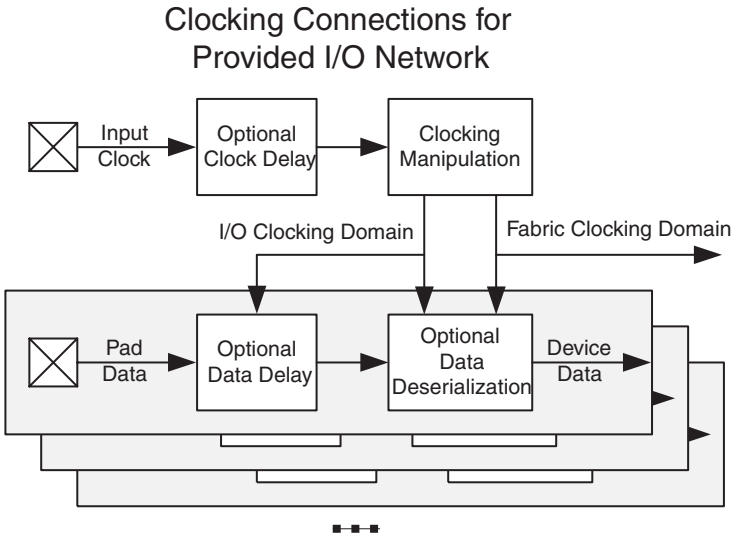

Figure 3-1: **Provided I/O Circuit**

I/O Datapath

The wizard assists the user in instantiating and configuring the components within the I/O interconnect block.

The user can choose to use delay insertion through an IODELAY2, or this functionality can be bypassed. Likewise, the user can choose to use serialization/deserialization through use of an ISERDES2 and/or OSERDES2, or they can register double data-rate data through use of an IDDR2 and/or ODDR2, or they can use the I/O registers for single rate data, or they can directly drive into fabric. The dataflow graph for an input bus is shown in Figure 3-2. For an output bus, the components will be similar, but the data will flow in the other direction. For a bidirectional bus, there will be both an input and output path, although there is only one IODELAY2 element.

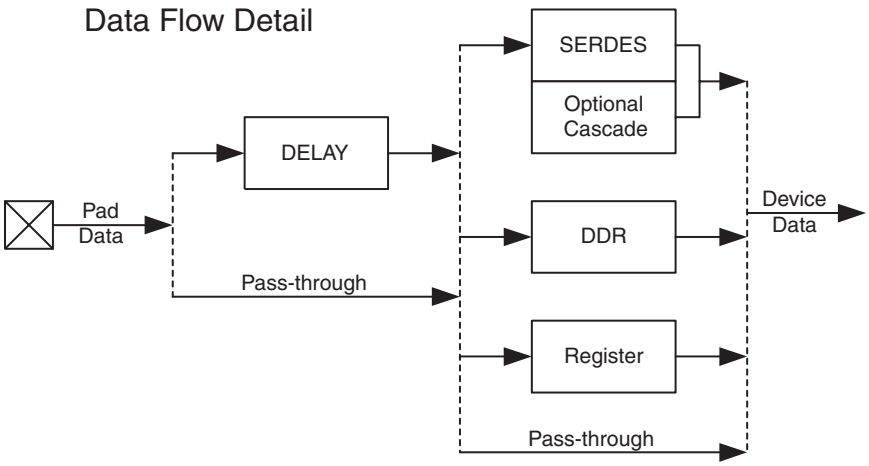

Figure 3-2: **Flow in the I/O Input Datapath**

I/O Signals

Table 3-1 describes the input and output ports provided by the I/O circuit. All ports are optional, although there will be at least one input clock, one signal tied to a pin connection, and one signal tied to a device connection. Availability of the ports is controlled by user-selected parameters. For example, when a variable delay is selected, the delay programming ports are exposed to the user. Any port is not exposed is tied off or connected to an open. For more information about specific I/O interconnect primitives, see the *Spartan-6 FPGA SelectIO Resources User Guide*. For more information about the specific I/O clock primitives, see the *Spartan-6 FPGA Clocking Resources User Guide*.

Table 3-1: **I/O Circuit Input and Output Port Descriptions**

Port	I/O	Description
Clock Ports [a]		
CLK_IN	Input	Clock in: Single-ended input clock. Available when a single-ended clock is selected.
CLK_IN_P	Input	Clock in Positive and Negative. Available when a differential clock source is selected.
CLK_IN_N		

Table 3-1: **I/O Circuit Input and Output Port Descriptions *(Cont'd)***

Port	I/O	Description
CLK_OUT	Output	Clock out: Buffered and/or delayed output clock to connect to fabric. Available when no serialization is selected, and the clock primitive is not a BUFPLL.
CLK_DIV_IN	Input	Clock divided in: Input clock for serialization in the I/O Logic. Available when serialization is chosen, and the clock primitive is BUFPLL.
CLK_DIV_OUT	Output	Clock divided out: Buffered and divided output clock to connect to fabric. Available when serialization is selected, and the clock primitive is a BUFIO2.
Reset Ports		
CLK_RESET	Input	Clock reset: Reset connected to clocking elements in the circuit.
IO_RESET	Input	I/O reset: Reset connected to all other elements in the circuit.
Pin Data Bus Ports		
DATA_IN_FROM_PINS	Input	Data in from pins: Single-ended input bus on the side of the pins.
DATA_IN_FROM_PINS_P	Input	Data in from pins positive and negative: Differential input bus on the side of the pins.
DATA_IN_FROM_PINS_N		
DATA_OUT_TO_PINS	Output	Data out to pins: Single-ended output bus on the side of the pins.
DATA_OUT_TO_PINS_P	Output	Data out to pins positive and negative: Differential output bus on the side of the pins.
DATA_OUT_TO_PINS_N		
DATA_TO_AND_FROM_PINS	Input/ Output	Data to and from pins: Single-ended bidirectional data bus on the side of the pins
DATA_TO_AND_FROM_PINS_P	Input/ Output	Data to and from pins positive and negative: Differential bidirectional data bus on the side of the pins.
DATA_TO_AND_FROM_PINS_N		
Device Data Bus Ports		
DATA_IN_TO_DEVICE	Output	Data in to device: Input bus on the side of the device.
DATA_OUT_FROM_DEVICE	Input	Data out from device: Output bus on the side of the device.
Control and Status Ports		
BITSLIP	Input	Bit slip: Enable bit slip functionality on input data. Available on a input datapath and when enabled.

Table 3-1: **I/O Circuit Input and Output Port Descriptions *(Cont'd)***

Port	I/O	Description
TRAIN	Input	Train: Enable the training pattern. The train function is a means of specifying a fixed output pattern that can be used to calibrate the receiver of the signal. This port allows the FPGA logic to control whether the output is the fixed training pattern or the output data from the pins. Available on a output datapath and when enabled.
TRISTATE_OUTPUT	Input	3-state Output: Disables the output path. This signal is synchronized with the input data. Available with a bidirectional datapath.
LOCKED_IN	Input	Locked In: The input clock generator has locked. Available with a BUFPLL. Connect to locked indicator from the PLL in the fabric.
LOCKED_OUT	Output	Locked Out: The BUFPLL has locked. Use this signal as the PLL locked indicator.
Variable Delay Ports		
DELAY_BUSY	Output	Delay busy: The variable delay circuity is still busy- don't change current state.
DELAY_CLK	Input	Delay clock: The clock used to control the variable delay circuitry. Most designs will have this connected to the divided/buffered clock for the I/O logic.
DELAY_CLOCK_CAL	Input	Delay clock calibrate: Trigger calibration on the delay for the clock.
DELAY_CLOCK_CE	Input	Delay clock enable: Enable a delay change event for the clock.
DELAY_CLOCK_INC	Input	Delay clock increment: Controls whether the delay is incremented (when asserted) or decremented (when deasserted) when the delay clock is enabled.
DELAY_DATA_CAL	Input	Delay data calibrate: Trigger calibration on the delay for the datapath.
DELAY_DATA_CE	Input	Delay data clock enable: Enable a delay change event for the datapath.
DELAY_DATA_INC	Input	Delay data increment: Controls whether the delay is incremented (when asserted) or decremented (when deasserted) when the delay clock is enabled.
Phase Detector Interface Ports		
PD_CLK	Input	Phase detector clock: The clock used to control the phase detector functionality. Is normally connected to CLK_DIV_OUT of the module.

Table 3-1: **I/O Circuit Input and Output Port Descriptions *(Cont'd)***

Port	I/O	Description
PD_BUSY	Output	Phase detection busy: The phase detector circuitry is busy; don't change the current state.
PD_DATA_INC	Input	Phase detector increment: Controls whether the phase is incremented (asserted) or decremented (deasserted).
PD_DATA_CE	Input	Phase detector clock enable: Enables the increment or decrement set by PD_DATA_INC.
PD_CAL_MASTER	Input	Master IODELAY2 calibration: Invokes the calibration sequence of master IODELAY2 element. (Required by simulation only)
PD_CAL_SLAVE	Input	Slave IODELAY2 calibration: Invokes the calibration sequence of slave IODELAY2 element.
PD_CAL_RST	Input	Reset calibration: Resets the input delays to half the value found during the calibration sequence.
PD_VALID	Output	Phase valid: Asserted when one or more valid edges are detected.
PD_INC_DEC	Output	Increment and decrement: Indicates whether to increment or decrement the delay line.

a. Only a single-ended or differential input clock is required. For a BUFG or BUFIO2, this comes from a pin. For a BUFPLL, this comes from fabric.

Generating the Core

This chapter describes the GUI and follows the same flow required to set up the I/O circuit. Tool tips are available in the GUI for most features; simply place your mouse over the relevant text, and additional information is provided in a pop-up dialog.

Data Bus Setup

Page 1 of the GUI (Figure 4-1) allows you to set up some general features for the data bus.

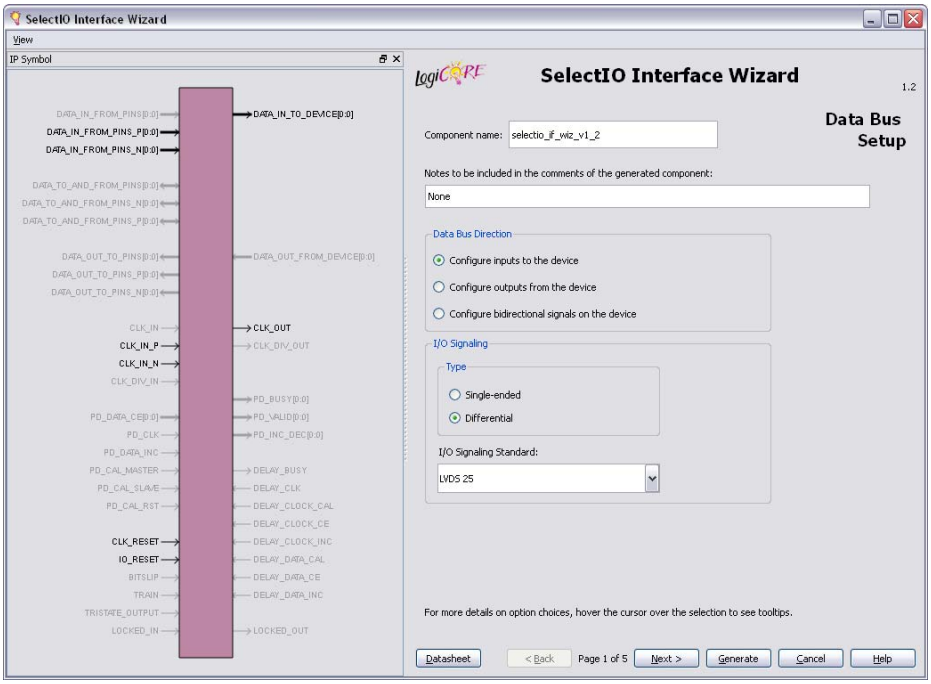

Figure 4-1: **Main Screen- Data Bus Setup - Page 1**

Component Name

User selectable component name and notes are available. Component names must not contain any reserved words in Verilog or VHDL. Notes must not include any spaces; instead use an underscore.

Data Bus Direction

The direction of the bus can be chosen here. Only choose bidirectional if you need your bus to be bidirectional: selecting it will cause restrictions later on in the configuration process.

I/O Signaling

Choose whether your bus is single-ended or differential. Single-ended signals with a serialization factor of 4 or less will occupy half of an I/O pair. Single-ended signals with a serialization factor of 5 or more will occupy an entire I/O pair. Differential signals will be created as I/O pairs.

All I/O signaling standards are shown for the I/O signaling type that has been selected. This value will appear in the generated HDL code.

Data Bus Setup 2

Page 2 of the GUI (Figure 4-2) allows you to specify the configuration for the I/O interconnect datapath.

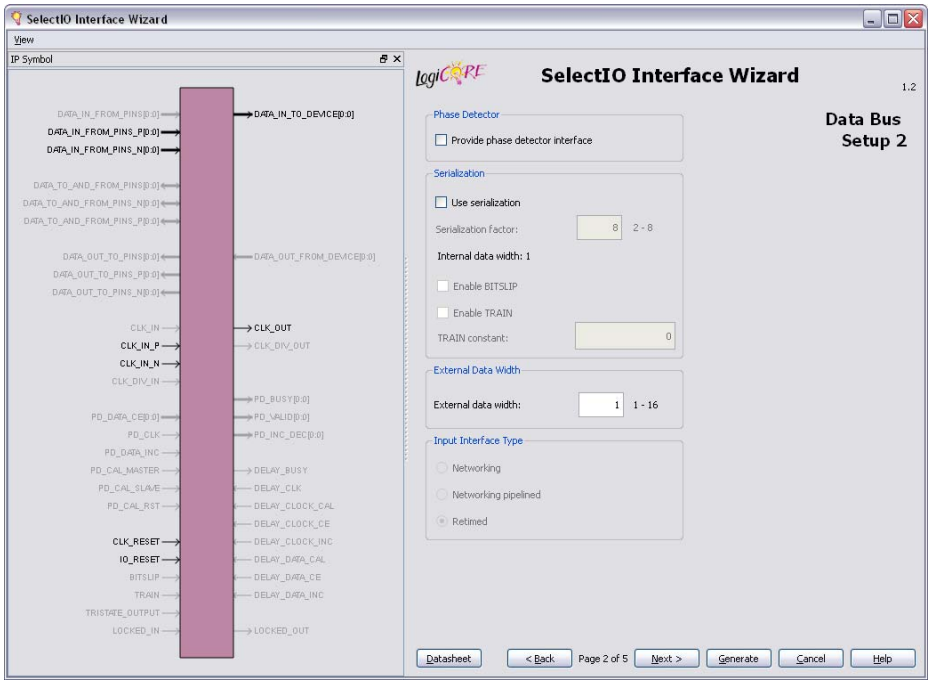

Figure 4-2: **Data Bus Setup - Page 2**

Phase Detector

If Provide Phase Detector Interface is selected, the IODELAY2 and ISERDES2 will be configured for phase detector. The bus on the device side will increase by the serialization factor. Selecting this feature also provides interface signals to the core, which can be used to interface a code that would control the phase detection. Selecting this option makes the wizard skip the Data Delay and Clock Delay pages. The Phase Detector box is available only when I/Os are configured as Inputs with differential I/O standard.

Serialization

If Use Serialization is selected, an ISERDES2 and/or OSERDES2 will be instantiated for the user. The bus on the device side will increase by the serialization factor. All data is collected by timeslice, then concatenated from right to left. For example, assume that the output data bus is 8-bits wide, with a serialization factor of 4. If the data is presented on the pins as: 00, 01, 02, and 03, the data presented to the device will be 03020100.

If a serialization factor of 5-8 is selected, two SERDES blocks per I/O will be instantiated for a user because each SERDES is capable of a maximum serialization of 4:1. Even if a single-ended bus was chosen, the entire I/O pair is now occupied. Once serialization is selected, BITSLIP and TRAIN can be chosen depending on the presence of an input or output datapath. The TRAIN constant will be configured in the source code.

If the Phase Detector interface is chosen, then both ISERDES2 are instantiated.

External Data Width

You can configure the number of bits on the system side, and this will automatically be set up on the device side. Note that differential signals will occupy two pins for each data bit.

Input Interface Type

If serialization is chosen, the interface type can be configured to set to specify the timing of the data on the device side.

Data Delay

Page 3 of the GUI (Figure 4-3) allows you to specify the type of delay for the data bus.

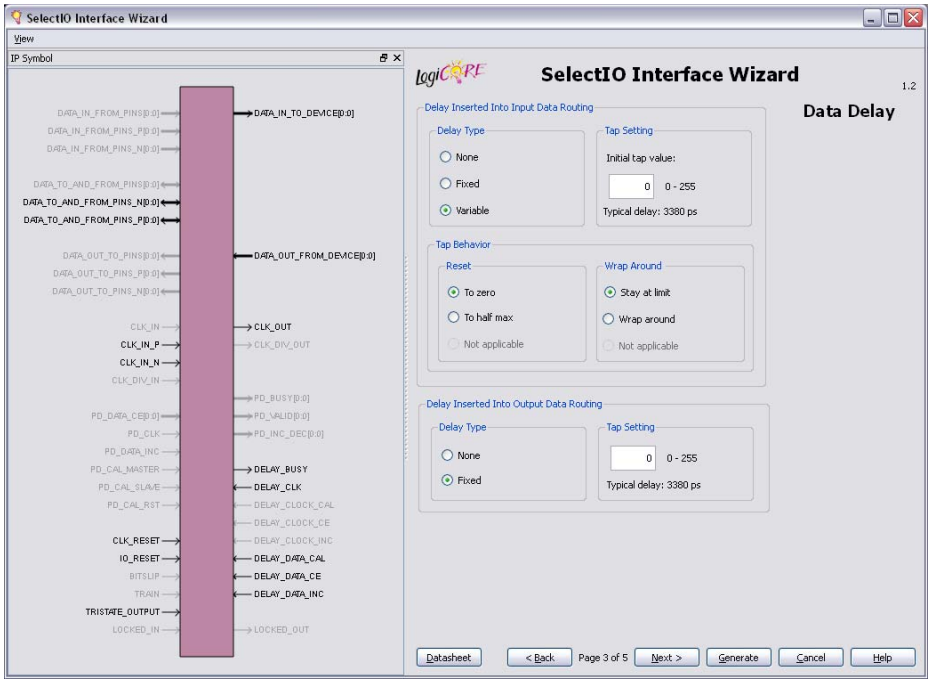

Figure 4-3: **Data Delay - Page 3**

Delay Type

An IODELAY2 will be instantiated if Fixed or Variable delay is chosen. Generally, if data is delayed with Fixed or Variable, delay will also be desired for the clock, given the high amount of insertion delay for the IODELAY2 primitive. The wizard will suggest delay settings for the clock based on the Data Delay settings. The tool will instantiate two IODELAY2 components when phase detector interface is chosen.

Tap Setting

If a delay is chosen, the tap value can be specified. A typical insertion delay for the value specified is show under the Tap value box. For a variable delay, the tap value is for the initial programming.

Tap Behavior

If a Variable delay is chosen, the user can specify the behavior during a reset/calibration sequence, and the behavior in the event the user attempts to go past the final value in the counter.

Clock Setup

Page 4 of the GUI (Figure 4-4) allows you to configure the behavior of the clock.

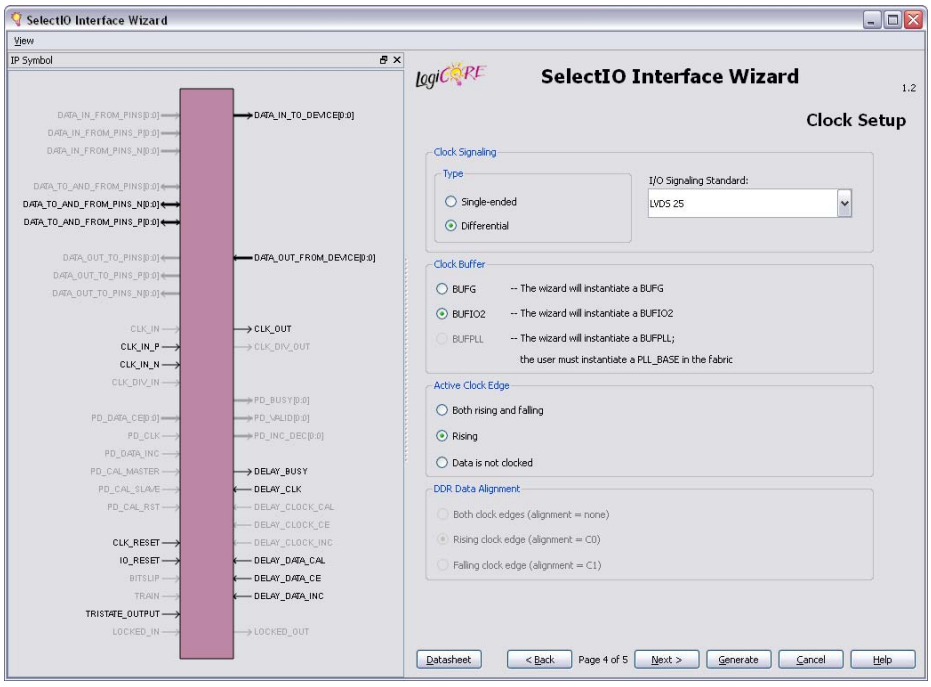

Figure 4-4: **Clock Setup - Page 4**

Clock Signaling

You can specify the signaling type and standard for the input clock. The I/O signaling standard will be embedded in the provided HDL source. Using double-data rate (DDR) data places some restrictions on clocks. Either a BUFIO2 with Differential signaling, or a BUFG with Single-ended or Differential signaling must be used in this case.

Clock Buffer

If your clock comes from a pin, you should leave the input buffer as a BUFIO2 for the most flexible functionality. In the event your clock comes from fabric, you will want to choose a BUFPLL, but you will need to be sure to instantiate a PLL_BASE in fabric to drive the BUFPLL. See the LogiCORE IP Clocking Wizard core and the *LogiCORE IP Clocking Wizard Getting Started Guide* for assistance with PLL_BASE instantiation and configuration.

Active Clock Edge

If using DDR data, select Both Rising And Falling. If the data requires an asynchronous delay only, select Data Is Not Clocked. In all other circumstances, leave it at the default value of Rising. If a topology is not available, you will not be able to select it. See the *Spartan-6 FPGA SelectIO Resources User Guide* and the *Spartan-6 FPGA Clocking Resources User Guide* for more information on clocking requirements.

DDR Data Alignment

If serialization is not chosen, but DDR data is chosen, the ODDR2 and IDDR2 primitives can be configured to align data to the rising, falling, or both edges of the input clock. Note that the internal data width will double, and that data will be grouped by timeslice just as is it for serialization.

Clock Delay

Page 5 of the GUI (Figure 4-5, page 24) allows you to specify the type of delay for the clock bus. Please see "Data Delay" for more information on the meanings of the fields within the clock delay configuration page. When using the Phase detector feature, the clock delay is set to FIXED with a tap value of 0.

- If there is no delay in the data path, there generally should not be any delay in the clock path, choose None.
- If there is delay in the data path, you'll generally want to match the insertion delay in the clock path, choose Fixed with a tap value of 0.

Other settings are made available to allow specific circuit topologies for expert users, but will not be used for a typical design.

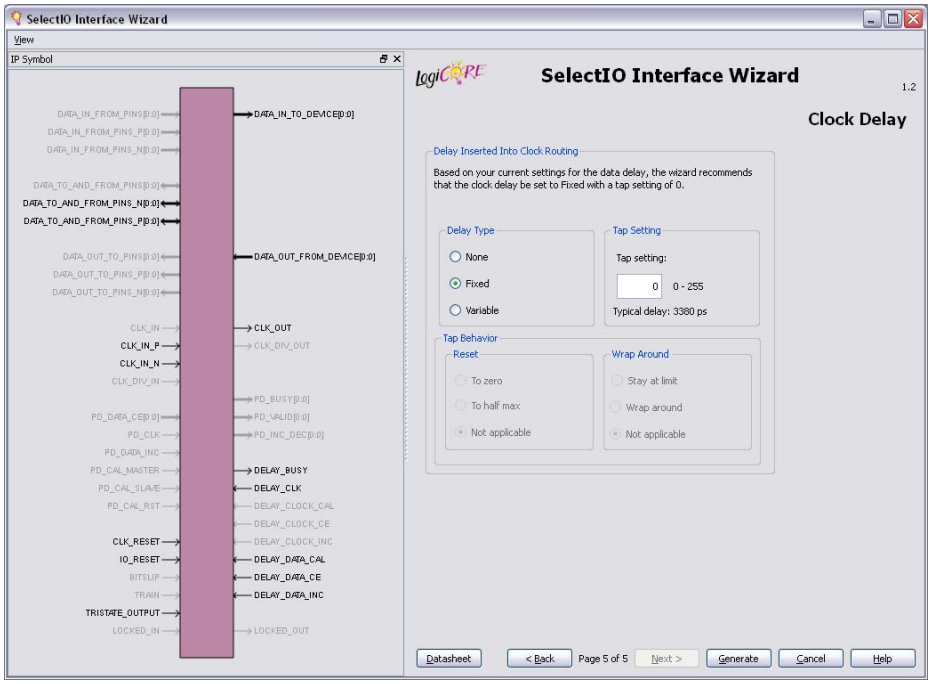

Figure 4-5: **Clock Delay**

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Chapter 5

Detailed Example Design

This chapter provides detailed information about the example design, including a description of files and the directory structure generated by the Xilinx® CORE Generator™ tool, the purpose and contents of the provided scripts, the contents of the example HDL wrappers, and the operation of the demonstration test bench.

- **<project directory>**
  Top-level project directory; name is user-defined
  - <project directory>/<component name>
    Core release notes file
    - <component name>/doc
      Product documentation
    - <component name>/example design
      Verilog and VHDL design files
    - <component name>/implement
      Implementation script files
      - implement/results
        Results directory, created after implementation scripts are run, and contains implement script results
    - <component name>/simulation
      Simulation scripts
      - simulation/functional
        Functional simulation files

Directory and File Contents

The SelectIO™ Interface Wizard core directories and their associated files are defined below.

<project directory>

The <project directory> contains all the CORE Generator tool project files.

Table 5-1: **Project Directory**

Name	Description
<project_dir>	
<component_name>.v[hd]	Verilog or VHDL source code.
<component_name>.xco	CORE Generator tool project-specific option file; can be used as an input to the CORE Generator tool.
<component_name>_flist.txt	List of files delivered with the core.
<component_name>.{veo|vho}	VHDL or Verilog instantiation template.
<component_name>.ise	Files used to incorporate the core into an ISE® software project.

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<project directory>/<component name>

The <component name> directory contains the release notes file provided with the core, which may include last-minute changes and updates.

Table 5-2: **Component Name Directory**

Name	Description
<project_dir>/<component_name>	
selectio_wizard_v1_1_release_notes.txt	SelectIO Interface Wizard release notes file.

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<component name>/example design

The example design directory contains the example design files provided with the core.

Table 5-3: **Example Design Directory**

Name	Description
<project_dir>/<component_name>/example_design	
<component_name>_exdes.v[hd]	Implementable Verilog or VHDL example design, connecting the I/O circuit to a RAM.

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<component name>/doc

The doc directory contains the PDF documentation provided with the core.

Table 5-4: **Doc Directory**

Name	Description
<project_dir>/<component_name>/doc	
selectio_wiz_ds746.pdf	*LogiCORE IP SelectIO Interface Wizard v1.2 Data Sheet*
selectio_wiz_gsg700.pdf	*LogiCORE IP SelectIO Interface Wizard v1.2 Getting Started Guide*

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<component name>/implement

The implement directory contains the core implementation script files.

Table 5-5: **Implement Directory**

Name	Description
<project_dir>/<component_name>/implement	
Scripts and projects to implement the example design	

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implement/results

The results directory is created by the implement script, after which the implement script results are placed in the results directory.

Table 5-6: **Results Directory**

Name	Description
<project_dir>/<component_name>/implement/results	
Implement script result files.	

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<component name>/simulation

The simulation directory contains the simulation test bench for the example design.

Table 5-7: **Simulation Directory**

Name	Description
<project_dir>/<component_name>/simulation	
<component_name>_tb.v	Demonstration test bench.

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simulation/functional

The functional directory contains functional simulation scripts provided with the core.

Table 5-8: **Functional Directory**

Name	Description
<project_dir>/<component_name>/simulation/functional	
Contains simulation scripts and waveform formats.	

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Implementation Scripts

The implementation script is either a shell script or batch file that processes the example design through the Xilinx tool flow. It is located at:

UNIX

```
<project_dir>/<component_name>/implement/implement.sh
```

Windows

```
<project_dir>/<component_name>/implement/implement.bat
```

The implement script performs the following steps:

- Synthesizes the HDL example design files using XST
- Runs Ngdbuild to consolidate the core netlist and the example design netlist into the NGD file containing the entire design
- Maps the design to the target technology
- Place-and-routes the design on the target device
- Performs static timing analysis on the routed design using Timing Analyzer (TRCE)
- Generates a bitstream
- Enables Netgen to run on the routed design to generate a VHDL or Verilog netlist (as appropriate for the Design Entry project setting) and timing information in the form of SDF files

The Xilinx tool flow generates several output and report files. These are saved in the following directory which is created by the implement script:

```
<project_dir>/<component_name>/implement/results
```

Simulation Scripts

Functional Simulation

The test scripts are a ModelSim, IUS, VCS, or ISIM macro that automate the simulation of the test bench. They are available from the following location:

```
<project_dir>/<component_name>/simulation/functional/
```

The test script performs the following tasks:

- Compiles the structural UniSim simulation model

- Compiles HDL Example Design source code
- Compiles the demonstration test bench
- Starts a simulation of the test bench
- Opens a Wave window and adds signals of interest
- Runs the simulation to completion

Example Design

Top Level Example Design

The following files describe the top-level example design for the SelectIO Interface Wizard core.

VHDL

```
project_dir>/<component_name>/example_design/<component_name>_exdes.vhd
```

Verilog

```
project_dir>/<component_name>/example_design/<component_name>_exdes.v
```

The top-level example design adds a RAM on the user side of the I/O. In the event that a BUFPLL is chosen as the clocking primitive, it also instantiates and configures the required PLL_BASE. This allows the entire design to be synthesized and implemented in a target device to provide post place-and-route gate-level simulation.

Customizing the Example Design

The example design features parameters such as RAM size. By changing the parameters, the RAM can be increased or decreased in size. Initialization values can also be added to the RAM in the example design, rather than requiring that the RAM be loaded with values during operation.

Demonstration Test Bench

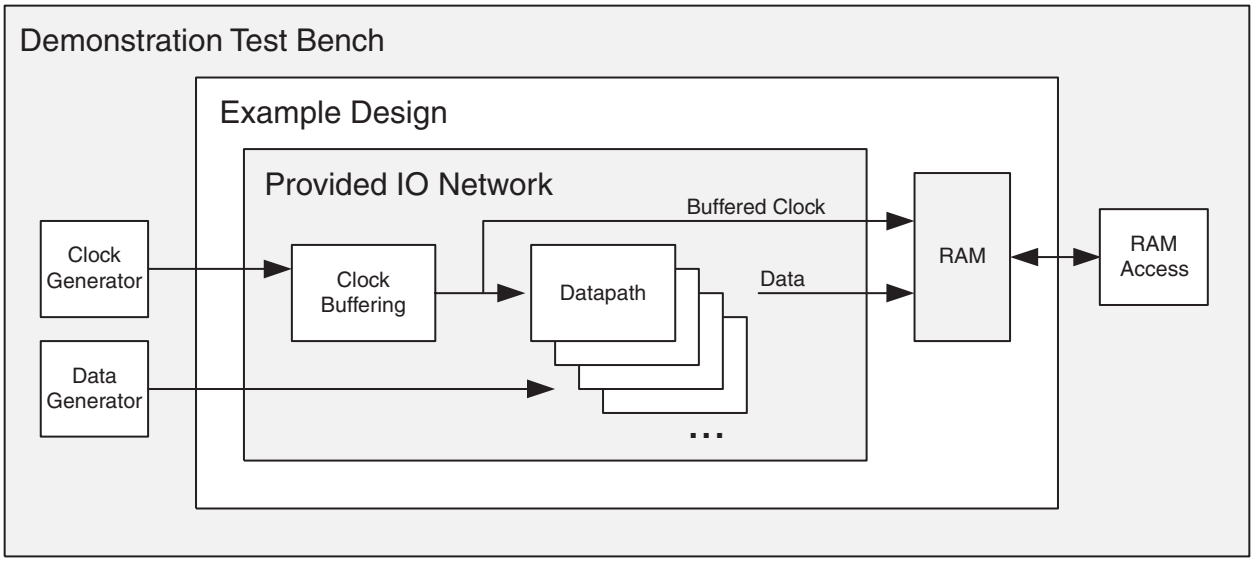

Figure 5-1: **Demonstration Test Bench for the SelectIO Interface Wizard Core and Example Design**

The following files describe the demonstration test bench.

VHDL

```
project_dir>/<component_name>/simulation/<component_name>_tb.vhd
```

Verilog

```
project_dir>/<component_name>/simulation/<component_name>_tb.v
```

The demonstration test bench is a simple VHDL or Verilog program to exercise the example design and the core.

The demonstration test bench performs the following tasks:

- Generates input clock signals
- Applies a reset to the example design
- For an output only design, the example design memory is pre-loaded with data
- For a design with an input path, data is driven onto the pins and received in the memory
- For a design with bidirectional ports, the I/O input logic is reconfigured to be outputs
- For a design with an output path, data read from the memory and driven out on the pins