LogiCORE IP Aurora 8B/10B v5.1

DS637 December 2, 2009 **Product Specification**

Introduction

The LogiCORE™ IP Aurora 8B/10B core implements the Aurora 8B/10B protocol using the high-speed serial transceivers on the Virtex®-5 LXT, SXT, FXT, and TXT family, the Virtex-6 LXT, SXT, CXT, and Lower Power family, and the Spartan®-6 LXT family.

The Aurora 8B/10B core is a scalable, lightweight, link-layer protocol for high-speed serial communication. The protocol is open and can be implemented by Aurora 8B/10B protocol licensees using any technology. The protocol is typically used in applications requiring simple, low-cost, high-rate, data channels.

The CORE Generator™ software produces source code for Aurora 8B/10B cores with variable datapath width. The cores can be simplex or full-duplex, and feature one of two simple user interfaces and optional flow control.

Features

- General purpose data channels with throughput range from 400 Mbps to 83.2 Gbps
- Supports up to any 16 of 48 Virtex-5 FPGA GTP/GTX transceivers or 16 of 36 Virtex-6 FPGA GTX transceivers or 4 of 8 Spartan-6 FPGA GTP transceivers
- Aurora 8B/10B protocol specification v2.0 compliant
- Low resource cost (see "Resource Utilization")
- Easy-to-use framing and flow control
- Automatically initializes and maintains the channel
- Full-duplex or simplex operation
- LocalLink (framing) or streaming user interface

LogiCORE IP Facts				
Core Specifics				
Supported Device Family	Virtex-5 LXT/SXT/FXT/TXT (1) Virtex-6 LXT/SXT/CXT, -1L (2) Spartan-6 LXT (3)			
Resources Used	I/O	LUTs	FFs	Block RAMs
	Varies with channel size See "Resource Utilization," page 8			0
Special Features	Open source; Core is free to use with Xilinx devices			
Provided with Core				
Documentation	Product Specification User Guide Getting Started Guide			
Design File Formats	Verilog and VHDL			
Constraints File	.ucf (user constraints file)			
Verification	Example Design and Test Bench			
Design Tool Requirements				
Xilinx® Implementation Tools	ISE® 11.4 (4)			
Verification	Mentor Graphics ModelSim v6.4b and above			
Simulation	Mentor Graphics ModelSim v6.4b and above			
Synthesis	XST 11.4			
Support				
Provided by Xilinx, Inc., www.xilinx.com/support				

1. For more information, see DS100, *Virtex-5 Family Overview*
2. For more information, see DS150, *Virtex-6 Family Overview*
3. For more information, see DS160, *Spartan-6 Family Overview*
4. ISE Service Packs can be downloaded at http://www.xilinx.com/support/download.htm

Functional Overview

The Aurora 8B/10B core is a lightweight, serial communications protocol for multi-gigabit links. It is used to transfer data between devices using one or many GTP/GTX transceivers. Connections can be *full-duplex* (data in both directions) or *simplex* (Figure 1).

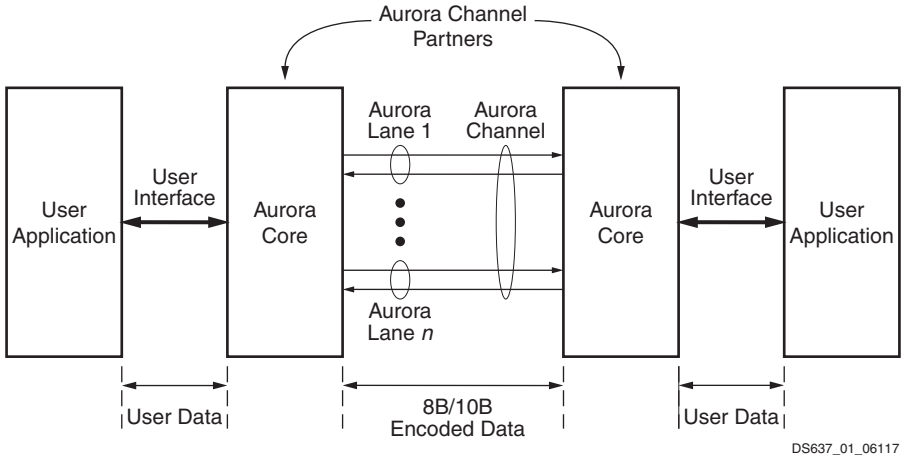

Figure 1: **Aurora 8B/10B Channel Overview**

Aurora 8B/10B cores automatically initialize a channel when they are connected to an Aurora channel partner. After initialization, applications can pass data freely across the channel as *frames* or *streams* of data. Aurora *frames* can be any size, and can be interrupted at any time. Gaps between valid data bytes are automatically filled with *idles* to maintain lock and prevent excessive electromagnetic interference. *Flow control* is optional in Aurora, and can be used to reduce the rate of incoming data, or to send brief, high-priority messages through the channel.

Streams are implemented in the Aurora 8B/10B core as a single, unending frame. Whenever data is not being transmitted, idles are transmitted to keep the link alive. The Aurora 8B/10B core detects single-bit, and most multi-bit errors using 8B/10B coding rules. Excessive bit errors, disconnections, or equipment failures cause the core to reset and attempt to re-initialize a new channel.

Applications

Aurora 8B/10B cores can be used in a wide variety of applications because of their low resource cost, scalable throughput, and flexible data interface. Examples of Aurora 8B/10B core applications include:

- **Chip-to-chip links**: Replacing parallel connections between chips with high-speed serial connections can significantly reduce the number of traces and layers required on a PCB. The core provides the logic needed to use GTP/GTX transceivers, with minimal FPGA resource cost.
- **Board-to-board and backplane links**: The Aurora 8B/10B core uses standard 8B/10B encoding, making it compatible with many existing hardware standards for cables and backplanes. Aurora 8B/10B cores can be scaled, both in line rate and channel width, to allow inexpensive legacy hardware to be used in new, high-performance systems.
- **Simplex connections (unidirectional)**: In some applications there is no need for a high-speed back channel. The Aurora protocol provides several ways to perform unidirectional channel initialization, making it possible to use the GTP/GTX transceivers when a back channel is not available, and to reduce costs due to unused full-duplex resources.

- **ASIC applications**: The Aurora protocol is not limited to FPGAs, and can be used to create scalable, high-performance links between programmable logic and high-performance ASICs. The simplicity of the Aurora protocol leads to low resource costs in ASICs as well as in FPGAs, and design resources like the Aurora bus functional model (ABFM 8B/10B) with compliance testing make it easy to get an Aurora channel up and running.

  Note: Contact Xilinx Sales or Auroramkt@xilinx.com for information on licensing the Aurora 8B/10B core for ASIC applications.

Functional Blocks

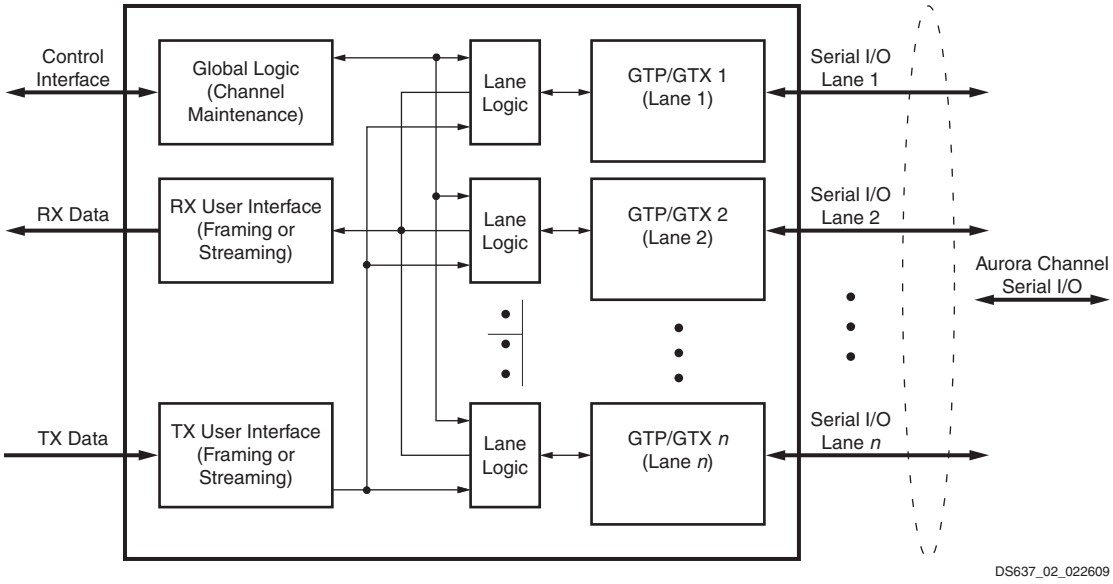

Figure 2: **Aurora 8B/10B Core Block Diagram**

Figure 2 shows a block diagram of the implementation of the Aurora 8B/10B core. The major functional modules of the Aurora 8B/10B core are:

- **Lane logic**: Each GTP/GTX transceiver is driven by an instance of the lane logic module, which initializes each individual GTP/GTX transceiver and handles the encoding and decoding of control characters and error detection.
- **Global logic**: The global logic module in each Aurora 8B/10B core performs the bonding and verification phases of channel initialization. While the channel is operating, the module generates the random idle characters required by the Aurora protocol and monitors all the lane logic modules for errors.
- **RX user interface**: The RX user interface moves data from the channel to the application. Streaming data is presented using a simple stream interface equipped with a data bus and a data valid signal. Frames are presented using a standard LocalLink interface. This module also performs flow control functions.
- **TX user interface:** The TX user interface moves data from the application to the channel. A stream interface with a data valid and a ready signal is used for streaming data. A standard LocalLink interface is used for data frames. The module also performs flow control TX functions. The module has an interface for controlling clock compensation (the periodic transmission of special characters to prevent errors due to small clock frequency differences between connected Aurora 8B/10B cores). This interface is normally driven by a standard clock compensation manager module provided with the Aurora 8B/10B core, but it can be turned off, or driven by custom logic to accommodate special needs.

Core Parameters

The users can customize Aurora 8B/10B cores by setting the parameters for the core using the CORE Generator software. Table 1 describes the customizable parameters. For examples of the GUI, see the *LogiCORE IP Aurora 8B/10B v5.1 Getting Started Guide* and the *LogiCORE IP Aurora 8B/10B v5.1 User Guide*.

Table 1: **Core Parameters**

Parameter	Description	Values Supported
Lanes	The number of GTP/GTX transceivers used in the channel.	Virtex-5 devices GTP/GTX: 1 to 16 Virtex-6 devices GTX: 1 to 16 Spartan-6 devices GTP: 1, 2, and 4
Lane Width	The Virtex-5 FPGA GTP transceivers in the core are set to use 2-byte fabric data. The Virtex-5/Virtex-6 FPGA GTX transceivers and Spartan-6 FPGA GTP transceivers in the core are set to use 2-byte as well as 4-byte SERDES.	Virtex-5 devices GTP: 2 bytes GTX: 2/4 bytes Virtex-6 devices GTX: 2/4 bytes Spartan-6 devices GTP: 2/4 bytes
Direction	The type of channel to be generated by the CORE Generator software. Can be full-duplex, simplex in the TX direction, simplex in the RX direction, or two separate simplex modules (one TX and one RX) sharing the same GTP/GTX transceivers.	Full-Duplex Simplex-TX Simplex-RX Simplex-Both
Backchannel	There are two types of Simplex Aurora 8B/10B cores: • Sidebands: Simplex TX state transition is through Sideband signals from the Simplex partner • Timer: Simplex TX state transition during initialization is achieved through a built-in Timer instead of sidebands	Sidebands Timer
Flow Control	Enables optional Aurora flow control. There are two types: • Native Flow Control (NFC): NFC allows full-duplex receivers to control the rate of incoming data. Completion mode NFC forces idles when frames are complete. Immediate mode NFC forces idles as soon as the flow control message arrives. • User Flow Control (UFC): UFC allows applications to send each other brief high priority messages through the channel.	None NFC Immediate NFC Completion UFC UFC and NFC Immediate UFC and NFC Completion
Interface	The user can specify one of two types of interfaces: • Framing: The framing user interface is LocalLink compliant. After initialization, it allows framed data to be sent across the Aurora channel. Framing interface cores tend to be larger because of their comprehensive word alignment and control character stripping logic. • Streaming: The streaming user interface allows users to start a single, infinite frame. After initialization, the user writes words to the frame using a simple register style interface with a data valid signal.	Framing (LocalLink) Streaming

Table 1: **Core Parameters *(Cont'd)***

Parameter	Description	Values Supported
Line Rate	The line rate dictates the speed at which the Transceiver works. This parameter relates to performance of the Aurora 8B/10B core. Choose the higher line rate for better performance. See the *LogiCORE IP Aurora 8B/10B v5.1 User Guide* for detailed instructions.	Virtex-5 devices GTP transceiver: 500 Mbps to 3.75 Gbps GTX transceiver: 750 Mbps to 6.5 Gbps Virtex-6 LXT/SXT devices GTX transceiver: 750 Mbps to 6.5 Gbps Virtex-6 CXT devices GTX transceiver: 750 Mbps to 3.75 Gbps Virtex-6 Lower Power devices GTX transceiver: 750 Mbps to 5.0 Gbps Spartan-6 devices GTP transceiver: 614 Mbps to 3.125 Gbps
Transceiver Reference Clock Frequency	The CORE Generator software accepts parameters to set the reference clock rate for Virtex-5, Virtex-6, and Spartan-6 FPGAs. See the *LogiCORE IP Aurora 8B/10B v5.1 User Guide* for detailed instructions.	A selection of legal rates based on the selected line rate and available clock multipliers in the: • Virtex-5 FPGA GTP/GTX transceivers • Virtex-6 FPGA GTX transceivers • Spartan-6 FPGA GTP transceivers
Transceiver Reference Clock	GTP/GTX transceivers can be fed a reference clock from a variety of dedicated and non-dedicated clock networks. See the *LogiCORE IP Aurora 8B/10B v5.1 User Guide* for instructions to select the best reference clock network for a given application.	Virtex-5 devices: GTPD/GTXD clocks Virtex-6 devices: GTXQ clocks Spartan-6 devices: GTPD clocks
Transceiver Placement	The CORE Generator software provides a graphical interface that allows users to assign lanes to specific GTP/GTX transceivers. The *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*, *Virtex-6 FPGA GTX Transceivers User Guide*, and *Spartan-6 FPGA GTP Transceivers User Guide* include guidelines for placing GTP/GTX transceivers for best timing results.	Any combination of GTP/GTX transceivers can be selected

Core Interfaces

The parameters used to generate each Aurora 8B/10B core determine the interfaces available (Figure 3) for that specific core. The Aurora 8B/10B cores have four to six interfaces:

- "User Interface," page 7
- "User Flow Control Interface," page 7
- "Native Flow Control Interface," page 7
- "Transceiver Interface," page 7
- "Clock Interface," page 7
- "Clock Compensation Interface," page 7

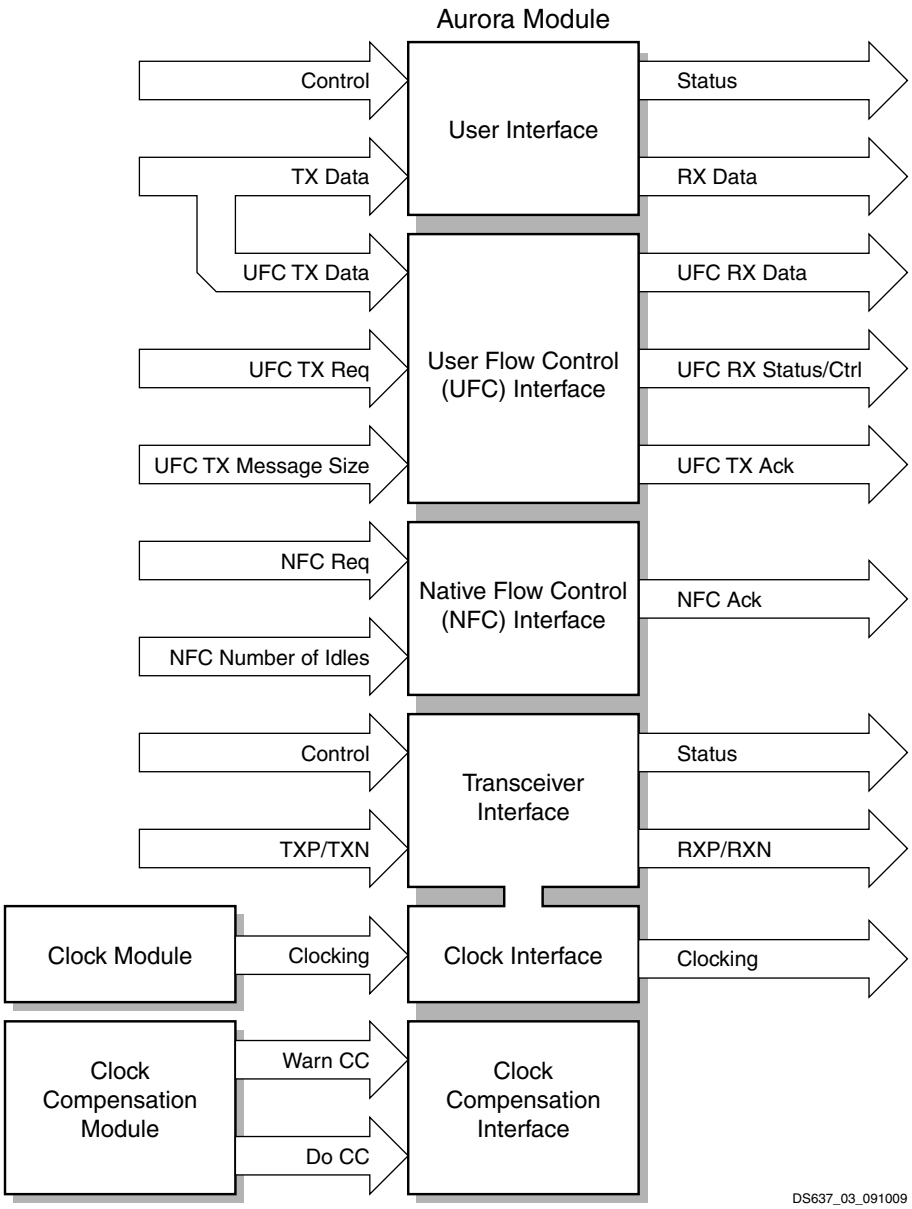

Figure 3: **Top-Level Interface**

User Interface

This interface includes all the ports needed to read and write *streaming* or *framed* data to and from the Aurora 8B/10B core. LocalLink ports are used if the Aurora 8B/10B core is generated with a framing interface; for streaming modules, the interface consists of a simple set of data ports and data valid ports. Full-duplex cores include ports for both transmit and receive; simplex cores use only the ports they require to send data in the direction they support. The width of the data ports in all interfaces depends on the number of GTP/GTX transceivers in the core, and on the width selected for these transceivers.

User Flow Control Interface

If the core is generated with user flow control (UFC) enabled, a UFC interface is created. The TX side of the UFC interface consists of a request and an acknowledge port that are used to start a UFC message, and a 3-bit port to specify the length of the message. The user supplies the message data to the data port of the user interface; immediately after a UFC request is acknowledged, the user interface indicates it is no longer ready for normal data, thereby allowing UFC data to be written to the data port.

The RX side of the UFC interface consists of a set of LocalLink ports that allows the UFC message to be read as a frame. Full-duplex modules include both TX and RX UFC ports; simplex modules retain only the interface they need to send data in the direction they support.

Native Flow Control Interface

If the core is generated with native flow control (NFC) enabled, an NFC interface is created. This interface includes a request and an acknowledge port that are used to send NFC messages, and a 4-bit port to specify the number of idle cycles requested.

Transceiver Interface

This interface includes the serial I/O ports of the GTP/GTX transceivers, and the control and status ports of the Aurora 8B/10B core. This interface is the user's access to control functions such as reset, loopback, channel bonding, clock correction, and powerdown. Status information about the state of the channel, and error information is also available here.

Clock Interface

This interface is most critical for correct Aurora 8B/10B core operation. The clock interface has ports for the reference clocks that drive the GTP/GTX transceivers, and ports for the parallel clocks that the Aurora 8B/10B core shares with application logic.

Clock Compensation Interface

This interface is included in modules that transmit data, and is used to manage clock compensation. Whenever the DO_CC port is driven High, the core stops the flow of data and flow control messages, then sends clock compensation sequences. For modules with UFC and NFC, the WARN_CC port prevents UFC messages and CC sequences from colliding. Each Aurora 8B/10B core is accompanied by a clock compensation management module that is used to drive the clock compensation interface in accordance with the *Aurora 8B/10B Protocol Specification*. When the same physical clock is used on both sides of the channel, WARN_CC and DO_CC should be tied Low. For more details about clock compensation, see the *LogiCORE IP Aurora 8B/10B v5.1 User Guide*.

Resource Utilization

Table 2 through Table 9 show the number of look-up tables (LUTs) and flip-flops (FFs) used in selected Aurora modules. The Aurora 8B/10B core is also available in configurations not shown in the tables; the estimated resource usage for these other modules can be extrapolated from the tables. These tables do not include the additional resource usage for flow control. These tables include the additional resource usage for the example design.

Table 2: **Virtex-5 LXT Family Resource Usage for Streaming**

Virtex-5 LXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	242	96	140	236
		FFs	275	141	152	287
2	2	LUTs	440	143	277	417
		FFs	519	246	300	538
4	2	LUTs	788	230	508	733
		FFs	965	444	552	988
8	2	LUTs	1495	788	979	1378
		FFs	1865	965	1058	1890
16	2	LUTs	2898	758	1913	2653
		FFs	3657	1633	2062	3686

Table 3: **Virtex-5 LXT Family Resource Usage for Framing**

Virtex-5 LXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	344	201	157	328
		FFs	382	177	200	395
2	2	LUTs	666	243	398	639
		FFs	751	324	453	769
4	2	LUTs	1200	369	779	1147
		FFs	1449	636	845	1473
8	2	LUTs	2609	619	1874	2486
		FFs	2779	1169	1663	2826
16	2	LUTs	6607	1109	5258	6348
		FFs	6072	2233	3877	6101

Table 4: **Virtex-5 SXT Family Resource Usage for Streaming**

Virtex-5 SXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	241	94	142	233
		FFs	275	140	149	283
2	2	LUTs	441	142	280	419
		FFs	519	243	294	531
4	2	LUTs	795	230	514	736
		FFs	965	441	542	977
8	2	LUTs	1492	397	968	1357
		FFs	1865	837	1046	1877
16	2	LUTs	2888	756	1884	2598
		FFs	3657	1630	2046	3670

Table 5: **Virtex-5 SXT Family Resource Usage for Framing**

Virtex-5 SXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	344	200	156	329
		FFs	382	179	197	391
2	2	LUTs	657	243	396	630
		FFs	751	322	447	763
4	2	LUTs	1203	373	782	1140
		FFs	1442	627	833	1454
8	2	LUTs	2583	617	1862	2475
		FFs	2763	1159	1623	2776
16	2	LUTs	6541	1124	5189	6275
		FFs	6064	2224	3859	6076

Table 6: **Virtex-5 FXT/TXT Family Resource Usage for Framing for 2-byte Lane Width**

Virtex-5 FXT/TXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	267	127	130	257
		FFs	276	122	162	284
2	2	LUTs	641	238	390	624
		FFs	716	286	447	727
4	2	LUTs	1184	363	767	1130
		FFs	1370	555	833	1382
8	2	LUTs	2591	616	1854	2470
		FFs	2619	1015	1622	2631
16	2	LUTs	6393	1112	5052	6153
		FFs	5777	1937	3860	5789

Table 7: **Virtex-5 FXT/TXT Family Resource Usage for Streaming for 2-byte Lane Width**

Virtex-5 FXT/TXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	241	92	139	227
		FFs	258	123	150	266
2	2	LUTs	432	136	274	410
		FFs	483	207	294	495
4	2	LUTs	784	221	503	721
		FFs	893	369	542	905
8	2	LUTs	1476	386	956	1340
		FFs	1721	693	1046	1733
16	2	LUTs	2814	717	1833	2545
		FFs	3370	1343	2047	3383

Table 8: **Virtex-5 FXT/TXT Family Resource Usage for Framing for 4-byte Lane Width**

Virtex-5 FXT/TXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	533	225	308	534
		FFs	633	260	393	645
2	4	LUTs	997	316	668	992
		FFs	1243	500	778	1272
4	4	LUTs	2246	521	1683	2198
		FFs	2340	907	1483	2385
8	4	LUTs	5866	928	4850	5768
		FFs	5228	1719	3587	5301
16	4	LUTs	17915	1745	15944	17672
		FFs	13450	3368	10219	13581

Table 9: **Virtex-5 FXT/TXT Family Resource Usage for Streaming for 4-byte Lane Width**

Virtex-5 FXT/TXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	316	124	193	318
		FFs	403	183	238	413
2	4	LUTs	610	177	388	564
		FFs	782	318	468	778
4	4	LUTs	1164	308	758	1065
		FFs	1469	592	877	1463
8	4	LUTs	2242	565	1482	2052
		FFs	2869	1142	1725	2860
16	4	LUTs	4313	1104	2884	4016
		FFs	5665	2257	3429	5679

Table 10: **Virtex-6 LXT Family Resource Usage for Framing for 2-byte Lane Width**

Virtex-6 LXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	441	244	206	456
		FFs	474	253	249	494
2	2	LUTs	793	346	524	862
		FFs	833	345	446	793
4	2	LUTs	1,398	488	951	1,431
		FFs	1,390	489	871	1,455
8	2	LUTs	2,914	800	2,040	2,834
		FFs	2,491	719	1,821	2,532
16	2	LUTs	7,320	1,359	5,780	7,078
		FFs	5,476	1,183	4,358	5,533

Table 11: **Virtex-6 LXT Family Resource Usage for Streaming for 2-byte Lane Width**

Virtex-6 LXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	316	179	154	326
		FFs	333	191	169	352
2	2	LUTs	517	250	267	516
		FFs	516	246	307	545
4	2	LUTs	876	382	478	865
		FFs	837	347	531	870
8	2	LUTs	1,588	656	893	1,537
		FFs	1,484	546	987	1,525
16	2	LUTs	3,173	1,177	1,746	2,885
		FFs	2,772	946	1,891	2,829

Table 12: **Virtex-6 LXT Family Resource Usage for Framing for 4-byte Lane Width**

Virtex-6 LXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	722	329	405	714
		FFs	741	314	468	763
2	4	LUTs	1,285	458	828	1,246
		FFs	1,275	432	892	1,308
4	4	LUTs	2,623	686	1,935	2,596
		FFs	2,240	612	1,686	2,281
8	4	LUTs	6,771	1,150	5,538	6,609
		FFs	4,985	971	4,087	5,042
16	4	LUTs	19,208	1,982	16,920	18,907
		FFs	12,654	1,692	11,068	12,743

Table 13: **Virtex-6 LXT Family Resource Usage for Streaming for 4-byte Lane Width**

Virtex-6 LXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	440	225	227	421
		FFs	426	216	249	446
2	4	LUTs	768	327	436	734
		FFs	717	294	468	746
4	4	LUTs	1,354	531	789	1,289
		FFs	1,238	443	844	1,271
8	4	LUTs	2,525	918	1,512	2,366
		FFs	2,290	743	1,604	2,331
16	4	LUTs	4,921	1,664	2,937	4,543
		FFs	4,386	1,344	3,116	4,443

Table 14: **Virtex-6 SXT Family Resource Usage for Framing for 2-byte Lane Width**

Virtex-6 SXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	435	235	205	433
		FFs	473	253	250	494
2	2	LUTs	768	333	452	776
		FFs	832	346	525	862
4	2	LUTs	1337	488	842	1410
		FFs	1397	488	952	1431
8	2	LUTs	2851	784	2044	2927
		FFs	2491	719	1823	2532
16	2	LUTs	7247	1332	5806	7360
		FFs	5475	1183	4359	5533

Table 15: **Virtex-6 SXT Family Resource Usage for Streaming for 2-byte Lane Width**

Virtex-6 SXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	297	160	155	306
		FFs	332	191	170	352
2	2	LUTs	502	231	273	492
		FFs	515	246	308	545
4	2	LUTs	868	369	473	832
		FFs	836	347	532	870
8	2	LUTs	1577	621	904	1518
		FFs	1483	546	988	1525
16	2	LUTs	3064	1155	1742	2900
		FFs	2771	946	1892	2829

Table 16: **Virtex-6 SXT Family Resource Usage for Framing for 4-byte Lane Width**

Virtex-6 SXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	686	287	393	670
		FFs	732	303	461	755
2	4	LUTs	1236	417	784	1180
		FFs	1265	424	884	1299
4	4	LUTs	2591	655	1904	2522
		FFs	2230	603	1678	2272
8	4	LUTs	6800	1095	5556	6621
		FFs	4975	963	4079	5033
16	4	LUTs	19437	2029	17033	19099
		FFs	12644	1683	11060	12734

Table 17: **Virtex-6 SXT Family Resource Usage for Streaming for 4-byte Lane Width**

Virtex-6 SXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	415	185	214	398
		FFs	417	205	242	438
2	4	LUTs	738	288	422	701
		FFs	708	287	460	738
4	4	LUTs	1307	481	778	1255
		FFs	1231	438	836	1265
8	4	LUTs	2484	815	1504	2349
		FFs	2287	745	1596	2329
16	4	LUTs	4824	1588	2934	4591
		FFs	4403	1350	3117	4458

Table 18: **Virtex-6 CXT Family Resource Usage for Framing for 2-byte Lane Width**

Virtex-6 CXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	431	234	204	442
		FFs	473	253	250	494
2	2	LUTs	771	328	452	776
		FFs	832	346	525	862
4	2	LUTs	1320	487	839	1402
		FFs	1397	488	952	1431
8	2	LUTs	2853	785	2057	2951
		FFs	2491	719	1823	2532
16	2	LUTs	7291	1341	5822	7410
		FFs	5475	1183	4359	5533

Table 19: **Virtex-6 CXT Family Resource Usage for Streaming for 2-byte Lane Width**

Virtex-6 CXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	301	164	155	311
		FFs	332	191	170	352
2	2	LUTs	502	232	272	493
		FFs	515	246	308	545
4	2	LUTs	847	375	475	843
		FFs	836	347	532	870
8	2	LUTs	1558	624	900	1524
		FFs	1483	546	988	1525
16	2	LUTs	3066	1162	1747	2914
		FFs	2771	946	1892	2829

Table 20: **Virtex-6 CXT Family Resource Usage for Framing for 4-byte Lane Width**

Virtex-6 CXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	689	290	392	674
		FFs	732	303	461	755
2	4	LUTs	1229	412	790	1183
		FFs	1265	424	884	1299
4	4	LUTs	2612	650	1924	2591
		FFs	2230	603	1678	2272
8	4	LUTs	6765	1090	5519	6624
		FFs	4977	963	4079	5035
16	4	LUTs	19425	2043	17078	19088
		FFs	12644	1683	11060	12734

Table 21: **Virtex-6 CXT Family Resource Usage for Streaming for 4-byte Lane Width**

Virtex-6 CXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	412	186	217	398
		FFs	417	205	242	438
2	4	LUTs	731	289	424	701
		FFs	708	287	460	738
4	4	LUTs	1323	486	786	1274
		FFs	1231	438	836	1265
8	4	LUTs	2516	815	1510	2379
		FFs	2287	745	1596	2329
16	4	LUTs	4865	1580	2959	4559
		FFs	4399	1350	3112	4458

Table 22: **Spartan-6 LXT Family Resource Usage for Framing for 2-byte Lane Width**

Spartan-6 LXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	418	223	197	413
		FFs	474	251	251	492
2	2	LUTs	747	337	441	738
		FFs	832	308	525	853
4	2	LUTs	1320	436	851	1282
		FFs	1397	471	952	1414

Table 23: **Spartan-6 LXT Family Resource Usage for Streaming for 2-byte Lane Width**

Spartan-6 LXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	288	154	147	287
		FFs	333	188	171	350
2	2	LUTs	481	210	260	465
		FFs	515	237	308	536
4	2	LUTs	824	327	455	775
		FFs	836	330	532	853

Table 24: **Spartan-6 LXT Family Resource Usage for Framing for 4-byte Lane Width**

Spartan-6 LXT Family			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	672	270	388	652
		FFs	732	300	461	752
2	4	LUTs	1235	385	788	1180
		FFs	1265	415	884	1290
4	4	LUTs	2555	575	1867	2461
		FFs	2230	587	1678	2255

Table 25: **Spartan-6 LXT Family Resource Usage for Streaming for 4-byte Lane Width**

Spartan-6 LXT Family			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	397	179	204	379
		FFs	417	203	242	435
2	4	LUTs	702	267	403	672
		FFs	708	278	460	729
4	4	LUTs	1248	431	723	1008
		FFs	1231	421	836	1248

Performance

The Aurora 8B/10B cores listed in Table 2, page 8 through Table 21, page 17 run at 156.25 MHz in devices with speed grades ranging from -1 to -3. For more details about performance and core latency, see the *LogiCORE IP Aurora 8B/10B v5.1 User Guide*.

Verification

Aurora 8B/10B cores are verified for protocol compliance using an array of automated hardware and simulation tests. The core comes with an example design implemented using a linear feedback shift register (LFSR) for understanding/verification of the core features.

The Aurora 8B/10B core is verified using the Aurora 8B/10B BFM and proprietary custom test benches. The Aurora 8B/10B BFM verifies the protocol compliance along with interface level checks and error scenarios. An automated test system runs a series of simulation tests on the most widely used set of design configurations chosen at random. Aurora 8B/10B cores are also tested in hardware for functionality, performance, and reliability using Xilinx GTP/GTX transceiver demonstration boards. Aurora verification testsuites for all possible modules are continuously being updated to increase test coverage across the range of possible parameters for each individual module.

Table 26: **Boards Used for Verification**

Test Boards
ML523
ML623
SP605

References

1. SP002, *Aurora 8B/10B Protocol Specification*
2. SP006, *LocalLink Interface Specification*
3. UG058, *Aurora 8B/10B Bus Functional Model User Guide* (Contact: auroramkt@xilinx.com)
4. UG352, *LogiCORE IP Aurora 8B/10B v5.1 Getting Started Guide*
5. UG353, *LogiCORE IP Aurora 8B/10B v5.1 User Guide*
6. UG196, *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*
7. UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*
8. UG366,*Virtex-6 FPGA GTX Transceivers User Guide*
9. UG386, *Spartan-6 FPGA GTP Transceivers User Guide*

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

The Aurora 8B/10B core is provided free of charge to licensed users. The licence for the Aurora 8B/10B core is also free and can be obtained by visiting www.xilinx.com/aurora.

There are three steps required to obtain the core:

1. Install Xilinx ISE 11.4. See the ISE product page for instructions if ISE software is not already installed.
2. Install Xilinx ISE 11.4 to add version 5.1 of the Aurora 8B/10B core to the list of cores available in the Core Selection window in the CORE Generator software. Instructions for this step are available in the *LogiCORE IP Aurora 8B/10B v5.1 Getting Started Guide*.
3. Electronically sign the Aurora 8B/10B Core License Agreement to obtain a license file for the Aurora 8B/10B core. Instructions for this step and the link to the page with the license and the CORE Generator software license file are also at www.xilinx.com/aurora. You must be a registered user on www.xilinx.com to sign the license.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/24/08	2.9	Initial Xilinx release.
03/24/08	2.9.1	Post-release updates and corrections.
06/27/08	3.0	Virtex-5 FPGA Aurora 3.0 release.
04/24/09	4.1	LogiCORE IP Aurora v4.1 release. Update tools to v11.1. Changed title of data sheet to not be device specific. Added support for Virtex-5 TXT family and Virtex-6 LXT family.
06/24/09	4.2	LogiCORE IP Aurora 4.2 release. Added support for the Virtex-6 CXT and SXT family.
12/02/09	5.1	LogiCORE IP Aurora 5.1 release. Added support for the Spartan-6 family.

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