## Introduction

The LogiCORE™ IP SelectIO™ Interface Wizard simplifies the integration of the SelectIO technology into the system design in the Spartan®-6 and Spartan-6 Lower Power devices. The Wizard creates an HDL file (Verilog or VHDL) that instantiates and configures I/O logic such as IOSERDES and IODELAY blocks configured to customer requirements. Additionally, it instantiates and configures the desired I/O clock primitive, connecting to the instantiated I/O logic.

## Features

- Supports input, output or directional busses
- Creates clock circuitry required to drive I/O logic
- Supports up to a 32-bit wide data bus
- Supports optional data serialization of up to 8 bits
- Supports optional data and/or clock delay insertion
- Supports single and double data rate data
- Supports single-ended or differential standards for both clock and or data
- Provides an optional interface to implement phase detector functionality
- Provides access to optional primitive ports
- Output can be pulled into PlanAhead™ design tools for further I/O attribute setting
- Provides synthesizable example design and demonstration test bench to help with integration

### LogiCORE IP Facts

| Core Specifics | | | | |
|---|---|---|---|---|
| Supported Device Family | Spartan®-6 Spartan-6 -1L | | | |
| Resources Used | I/O | LUTs | FFs | Block RAMs |
| | 1-33 | 0 | 0-16 | 0 |
| Special Features | Depending on user selection 0-18 IODELAY2, 0-32 ISERDES2, 0-32 OSERDES2, 0-16 ODDR, 0-16 IDDR, 0-2 BUFIO2, 0-1 BUFPLL, 1-3 BUFG | | | |

| Provided with Core | |
|---|---|
| Documentation | Product Brief Getting Started Guide |
| Design File Formats | Verilog, VHDL |
| Verification | Verilog, VHDL Test Bench |
| Instantiation Template | Verilog, VHDL Wrapper |

| Design Tool Requirements | |
|---|---|
| Xilinx Implementation Tools | ISE® 11.4 |
| Verification | Mentor Graphics ModelSim v6.4b and above, Cadence IUS v81 -s009 and above, Synopsys VCS and VCS MX 2008.09 and above Xilinx® ISIM |
| Simulation | Mentor Graphics ModelSim v6.4b and above Cadence IUS v81 -s009 and above Synopsys VCS and VCS MX 2008.09 and above Xilinx® ISIM |
| Synthesis | ISE tools, XST |

| Support | |
|---|---|
| Provided by Xilinx, Inc. | |

## Ordering Information

This SelectIO Interface Wizard is provided under the <u>SignOnce IP Site License</u>.

## Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|------|---------|--------------------------|
| 09/16/09 | 1.1 | Initial Xilinx release. |
| 12/02/09 | 1.2 | Added Spartan-6 -1L (Lower Power) device support. |

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