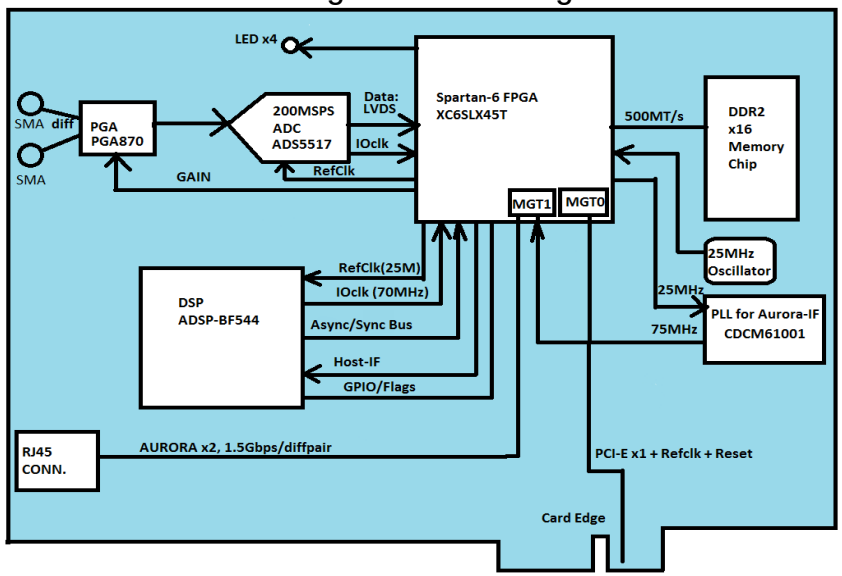
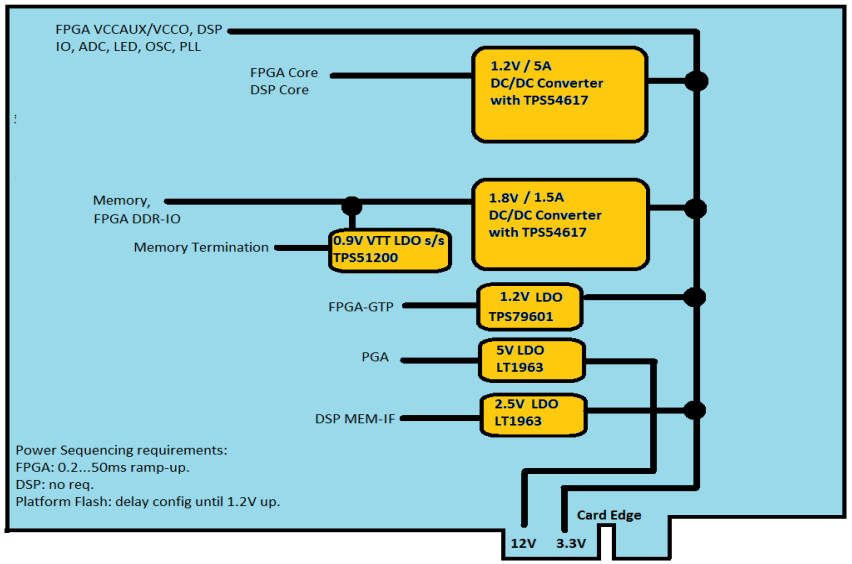
S6BF-BOARD (Spartan-6/Blackfin)

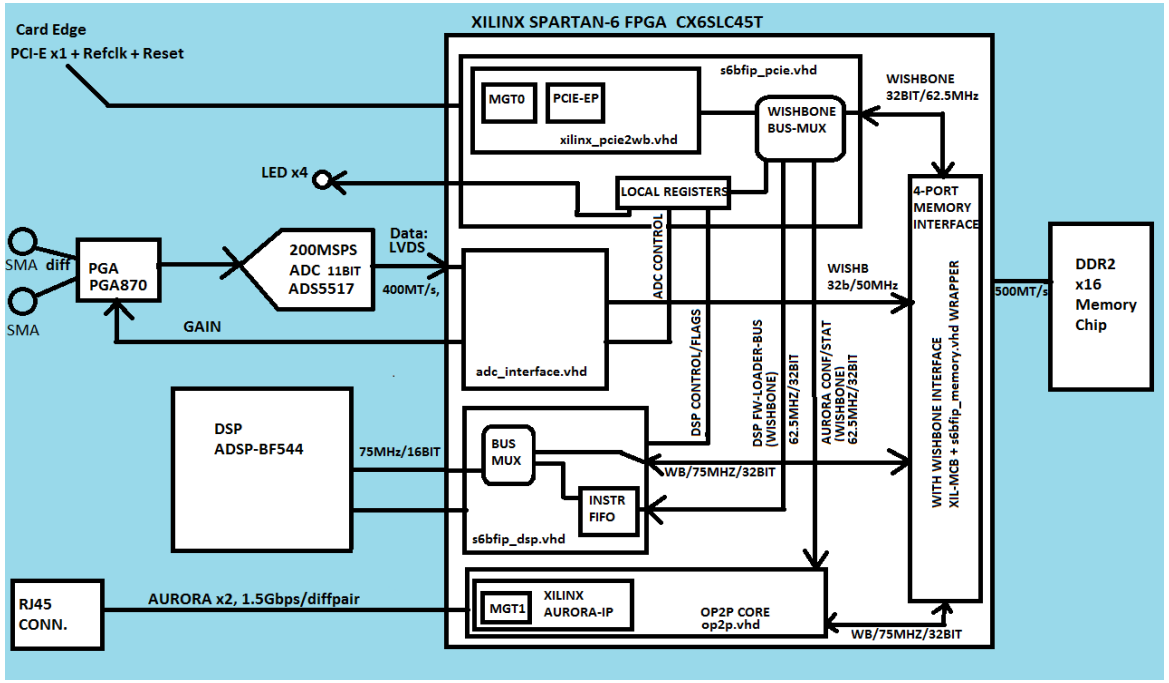
I/O and Clocking Block Diagram



Power Rails on the Board



FGPA Logic Block Diagram



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FPGA MAIN PAGE

MULTI-GIGABIT CONNECTIONS

CALIBRATION FOR BOTH GTPS
Match traces from R to FPGA.

AURORA CONNECTOR

CAT6 Crossover:
D1-D2, D3-D4
So, use it this way:
D1=TX0, D2=RX0, D3=TX1, D4=RX1

CON1 — RJ45 with CAT6 — RJ45_3004CF6101

MGT-PINS

XC6SLX45T-2FGG484C-S6BFBOARD

PCI-EXPRESS

U2 — PCIE_X1_CARD_EDGE

PCIE Signal Names are Relative to Host

CAP ON THE MB

CAP AT CONN

CAP AT LOAD

MEMORY INTERFACE VREF

UNUSED I/O PINS

VTEMP??? FROM REF.DESIGN

This reset may be used for detecting card edge hot reset. Normally the FPGA uses internal cold reset to initialize after the 400ms configuration time.

NOT CONNECTED

PCB RULES

(AURORA/DP2P INTERFACE)
PLACE CAPS CLOSE TO CONNECTOR
ROUTE DIFFPAIRS AT 100R_DIFF IMPEDANCE
LANE-TO-LANE SKEW MAX 50M
PHASE TOLERANCE: <0.125MM
CLEARANCE: 5H RULE

PCB RULES

(PCI-EXPRESS)
ROUTE DIFFPAIRS AT 100R_DIFF IMPEDANCE
PHASE TOLERANCE: <0.125MM
CLEARANCE: 5H RULE
CAP PLACEMENT: PCIE:AT CONN, REFCLK:AT CHIP

FPGA SYSTEM SIGNALS, JTAG/CONFIG

JTAG CONN

CON2 — 2X7_2MMPITCH_PINHEADER

TO FLASH

SYS-PINS

U3 — PLATFORM FLASH — XCF16PVOG48C

Some Config pins may toggle during the FPGA Config cycle.
These are: M20, N20, N19, AB5, T20.
In this design they are not connected to any external drivers, so its safe.

8-bit SELECTMAP config method is used.

TERMINATION AT FLASH INPUT

FPGA Power + Decap

POWER-PINS

GND-PINS

XC6SLX45T-2FGG484C-S6BFBOARD

APPLICATION SPECIFIC SYSTEM SIGNALS

SYS-PINS2

25MHz-->75MHz PLL
for Aurora GTP RefCLK

U4 — CDCM61001 — Freq is set by FPGA

XTAL1 25MHZ

CAP AT FPGA

Out=LVDS

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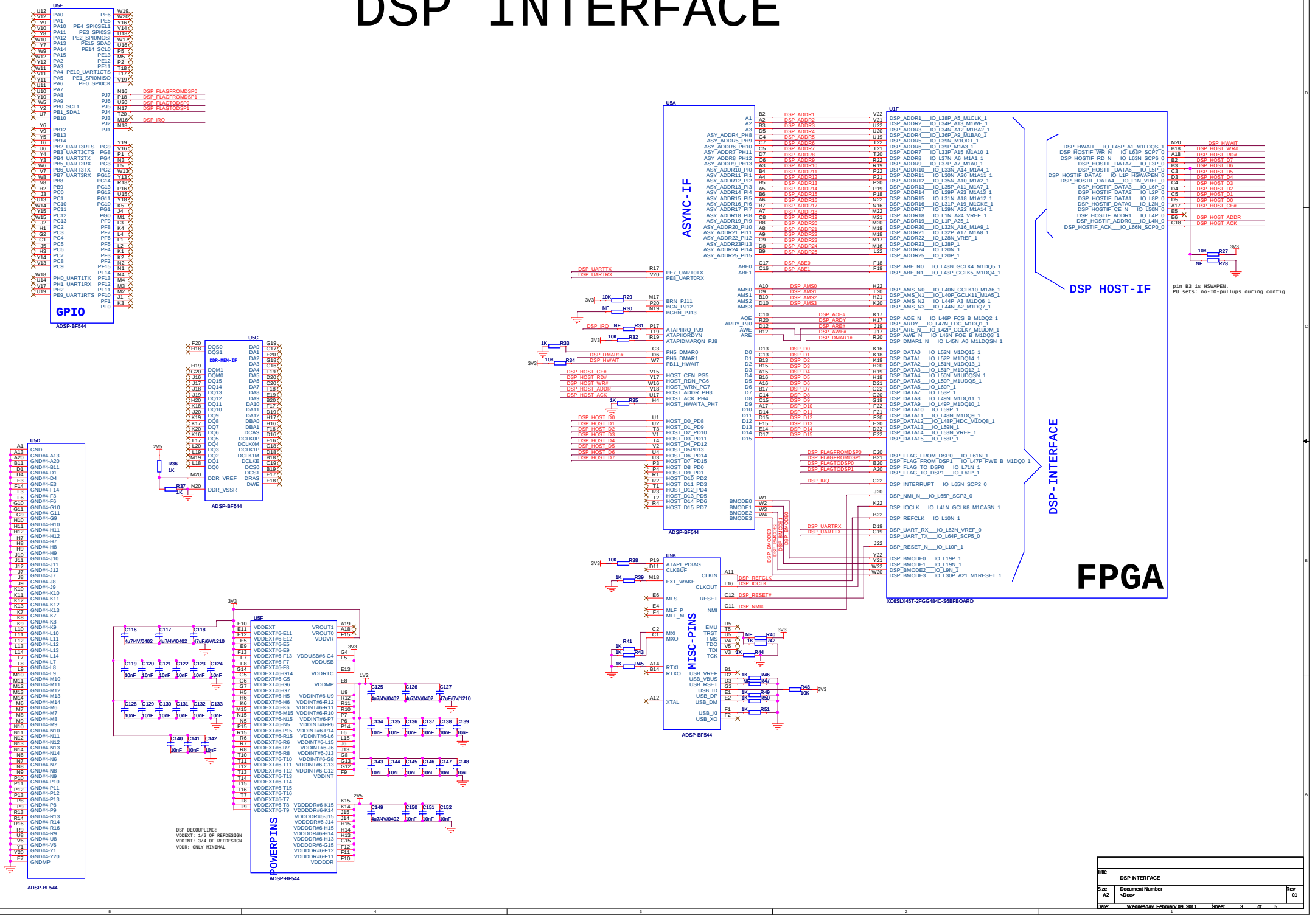
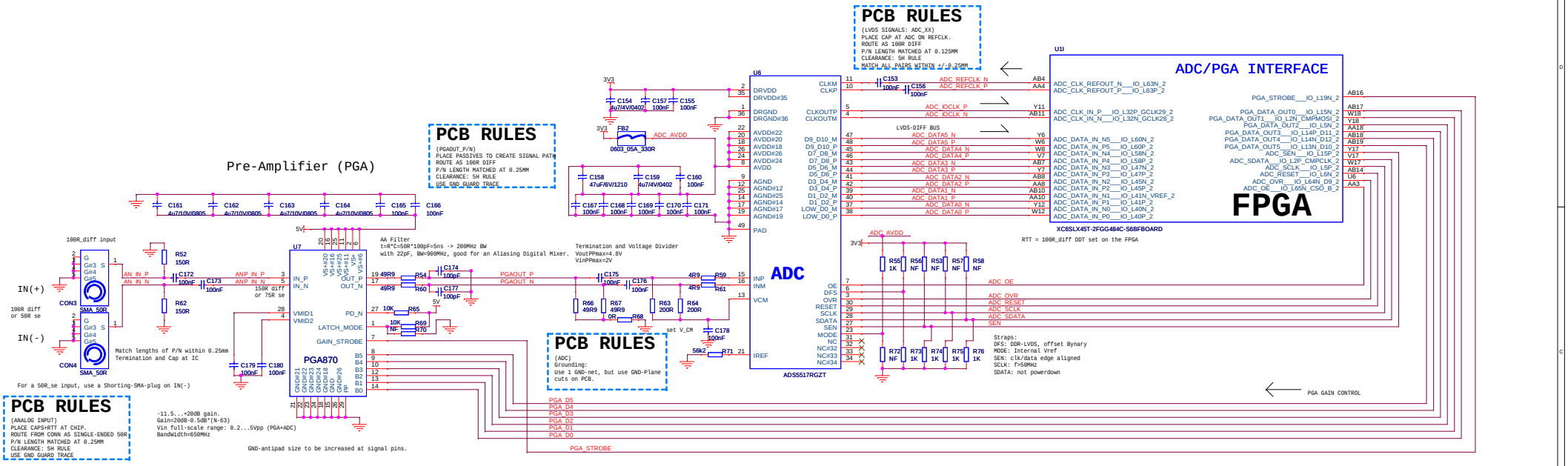
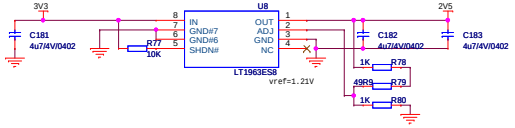
DSP INTERFACE



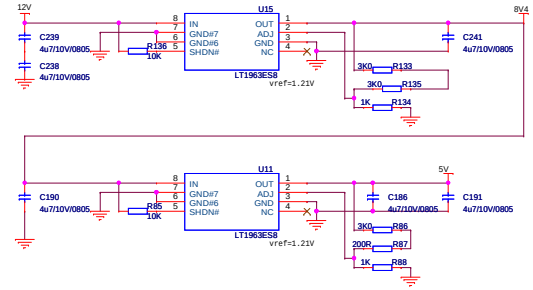
ANALOG CIRCUITS



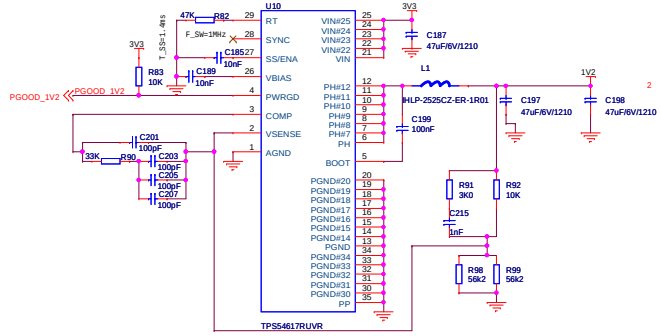
2.5V LDO FOR DSP-MEMIF



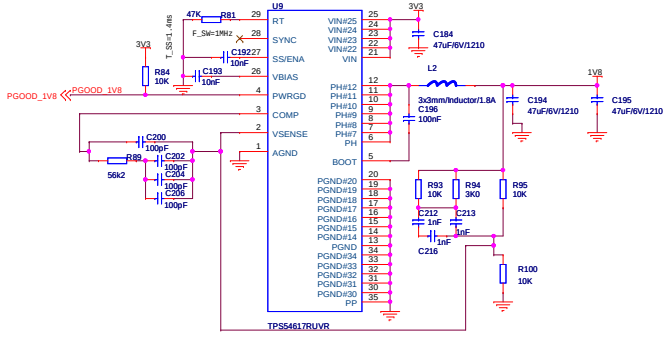
5V LDO FOR PGA (2 STAGES TO SHARE POWER)



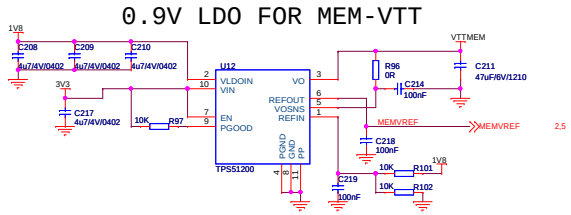
1.2V SWITCHING REGULATOR



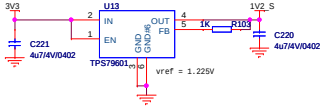
1.8V SWITCHING REGULATOR



0.9V LDO FOR MEM-VTT



1.2V LDO FOR GTP



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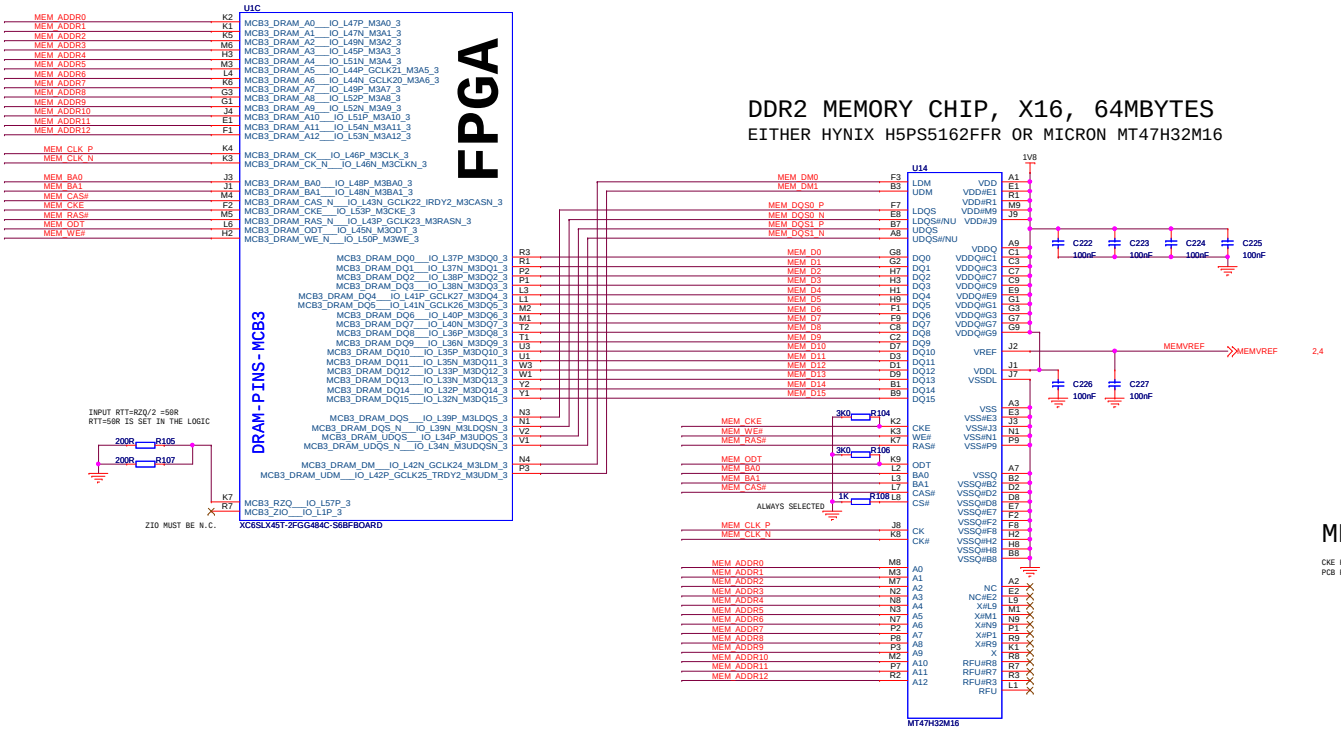
MEMORY INTERFACE



DDR2 MEMORY CHIP, X16, 64MBYTES

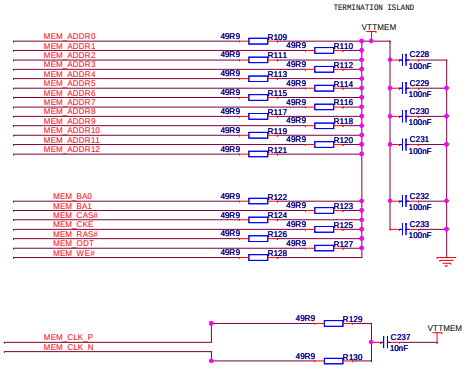
EITHER HYNIX H5PS5162FFR OR MICRON MT47H32M16

PCB RULES

```
(MEMORY INTERFACE: MEM_XX)
IMPEDANCE: SE=50R, DIFF=100R WITHOUT SE SPEC
DIFFPAIR PHASE TOLERANCE: 0.125MM
DATA LANE MATCH: +/-0.25MM, [15:8], [7:0]
ACC BUS MATCH: TO CLK WITHIN 5.5MM
ACC/CLK TOPOLOGY:  FPGA----MEM----RTT
CLK TO DQS MATCH: WITHIN 5.5MM
USE VTT ISLAND FOR RTT
LENGTH MATCHING IS DEFINED ON THE CHIP-TO-CHIP BASIS.
SPACING: 2H ON 70% OF LENGTH
```

MEMORY ACC-BUS TERMIANTION

CKE HAS NO TERMINATION
PCB ROUTING IS 50R, SO IS RTT



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